Schematics Page Index (Title / Revision / Change Date)

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11	PCH (PCI-E,SMBUS,CLK)	SA		53	Bluetooth Connector	SA			
12	PCH (DMI,FDI,GPIO)	SA		54	Felica Connector	SA			
13	PCH (LVDS,DDI)	SA		55	Status LED & LID	SA			
14	PCH (PCI,USB,NVRAM)	SA		56	FAN	SA			
15	PCH (GPIO,VSS_NCTF,RSVD)	SA		57	Touch Pad	SA			
16	PCH (POWER) 1/2	SA		58	Thermal Sensor	SA			
17	PCH (POWER) 2/2	SA		59	Switch DB Conn.	SA			
18	PCH (VSS)	SA		60	AUDIO SPEAKER CONNECTOR	SA			
19	CLOCK GEN	SA		61	Audio/USB DB Conn.	SA			
20	DDRIII(SO-DIMM 0) 1/3	SA		62	Switch (Botton & KB LED)	SA			
21	DDRIII(SO-DIMM 1) 2/3	SA		63	Audio (CODEC)	SA			
22	VGA (PCI-E) 1/6	SA		64	Audio (MUTE)	SA			
23	VGA (Strap) 2/6	SA		65	Audio (Power)	SA			
24	VGA (I/O) 3/6	SA		66	Audio (Audio & USB Conn.)	SA			
25	VGA (Memory BUS) 4/6	SA		67	Audio (Head Phone Jack)	SA			
26	VGA (LVDS) 5/6	SA		68	Audio (Ext MIC Jack)	SA			
27	VGA (Power) 6/6	SA		69	Audio (USB Port)	SA			
28	VRAM(DDR3)# 1/4	SA		70	Power Design Diagram	SA			
29	VRAM(DDR3)# 2/4	SA		71	DCIN&Charger	SA			
30	VRAM(DDR3)# 3/4	SA		72	Discharge Circuit	SA			
31	VRAM(DDR3)# 4/4	SA		73	Identify IC	SA			
32	VRAM(BYPASS) 1/2	SA		74	SYS Power (+3_3V/+5V)	SA			
33	VRAM(BYPASS) 2/2	SA		75	VTT&PCH Power(+1_1/1_05V)	SA			
34	CRT	SA		76	DDR3 Power(+1_5V/+0_75V)	SA			
35	LVDS	SA		77	SYS Power(+1_8V)	SA			
36	Inverter CONNECTOR	SA		78	CPU Power VHCORE	SA			
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38	HDMI	SA		80	VGA Power(ATI VDD)	SA			
39	EC+KBC (NPCE783L)	SA		81	Others power plane	SA			
40	KB Connector	SA		82	OVP protection	SA			
41	SPI Flash ROM	SA		83	HOLE & AMI LABEL	SA			
42	Debug Port	SA		84	History(1)	SA			

Project Code & Schematics Subject: **M960&M970 H Model**

PCB P/N:
1P-0099J00-80SB (IRIS MB)
1P-1099J00-80SB (IRIS AUDIO)
1P-1099J01-80SB (IRIS PWR)
1P-0099500-80SB (HANNSTAR MB)
1P-1099500-80SB (HANNSTAR Audio)
1P-1099501-80SB (HANNSTAR PWR)

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P. Leader	Check by	Design by

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Title: *Index Page*

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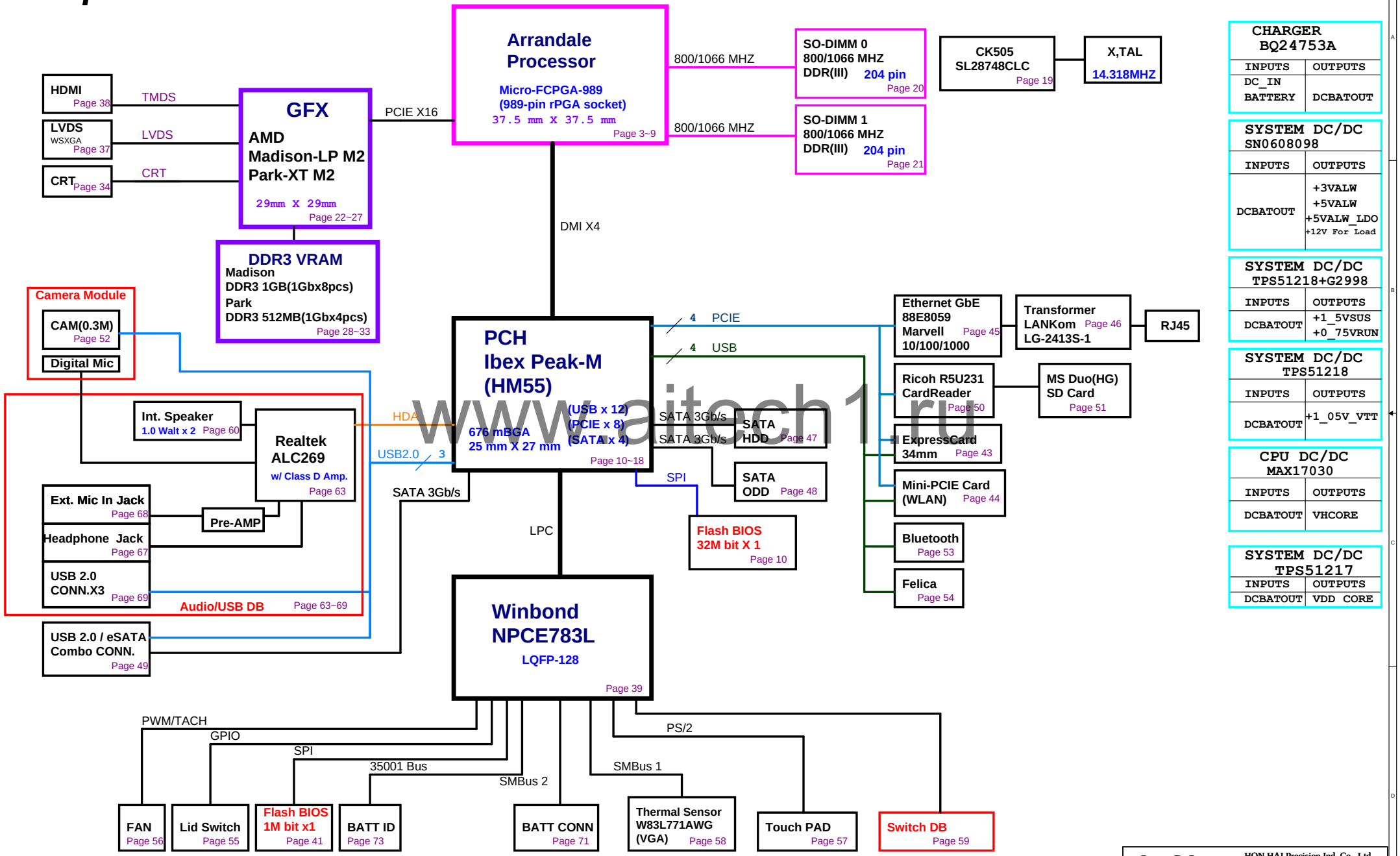
M960&M970 H Model Calpella Platform+ AMD Madison/Park Discrete Graphic+ VRAM*8



CHARGER BQ24753A	
INPUTS	OUTPUTS
DC_IN BATTERY	DCBATOUT

SYSTEM DC/DC SN0608098	
INPUTS	OUTPUTS
DCBATOUT	+3VALW +5VALW +5VALW_LDO +12V For Load

SYSTEM DC/DC TPS51218+G2998	
INPUTS	OUTPUTS
DCBATOUT	+1_5VSUS +0_75VRUN

SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
DCBATOUT	+1_05V_VTT

CPU DC/DC MAX17030	
INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC TPS51217	
INPUTS	OUTPUTS
DCBATOUT	VDD CORE

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Title: Block Diagram
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Rev: SA
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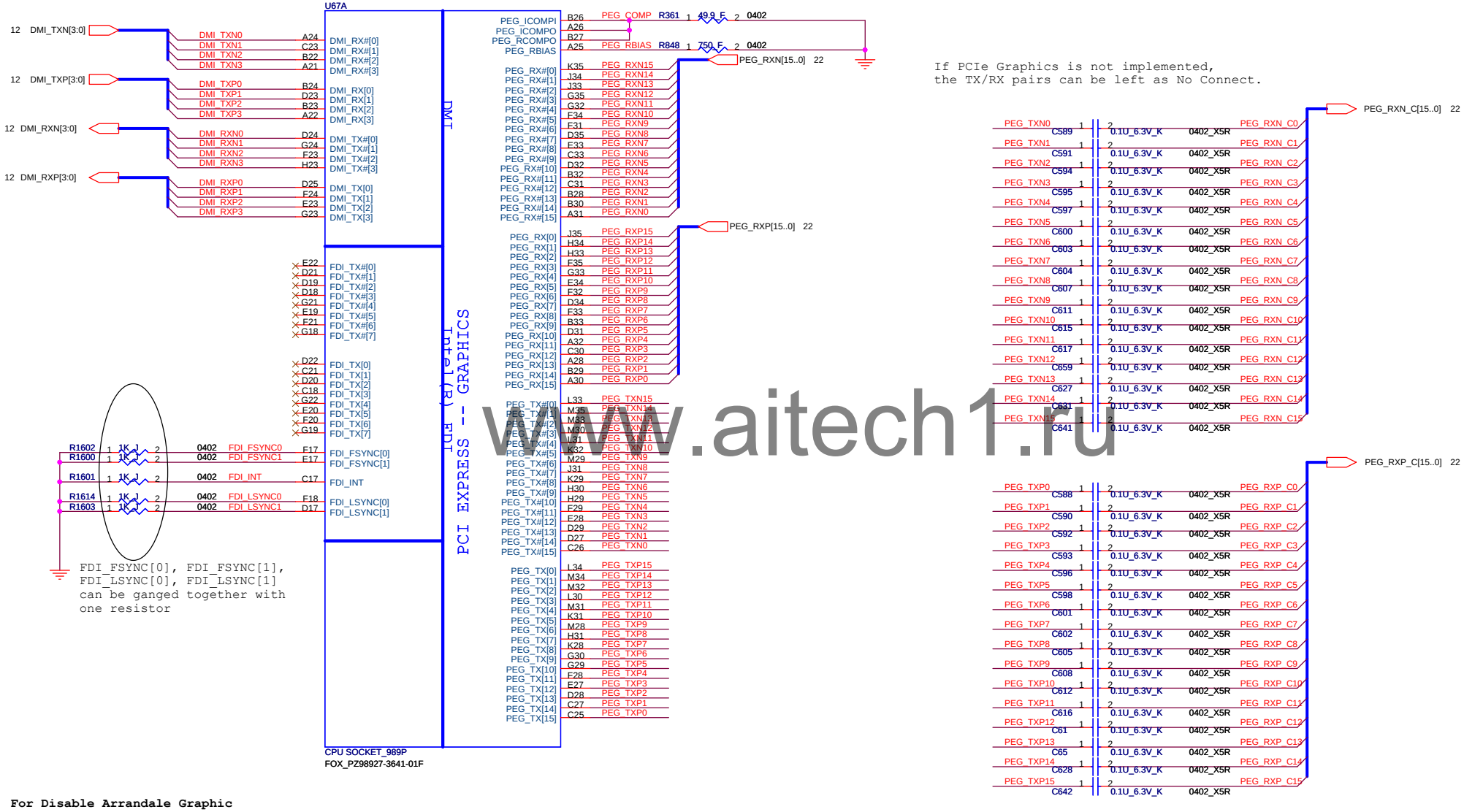

If PCIe Graphics is not implemented,
the TX/RX pairs can be left as No Connect.

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For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).
FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with
one resistor.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (DMI,PEG,FDI)	
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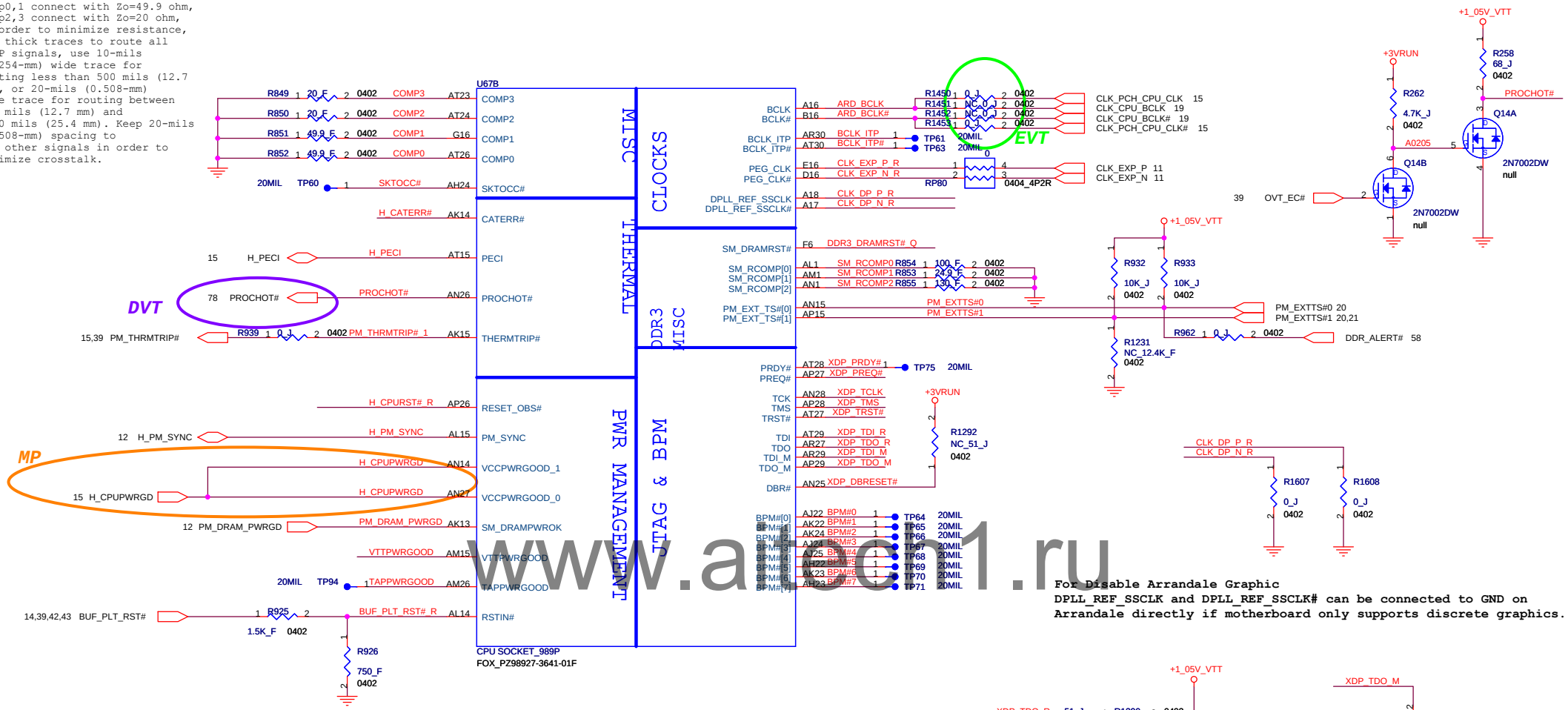
Layout Note:
Comp0,1 connect with Zo=49.9 ohm,
Comp2,3 connect with Zo=20 ohm,
In order to minimize resistance,
use thick traces to route all
COMP signals, use 10-mils
(0.254-mm) wide trace for
routing less than 500 mils (12.7
mm), or 20-mils (0.508-mm)
wide trace for routing between
500 mils (12.7 mm) and
1000 mils (25.4 mm). Keep 20-mils
(0.508-mm) spacing to
any other signals in order to
minimize crosstalk.



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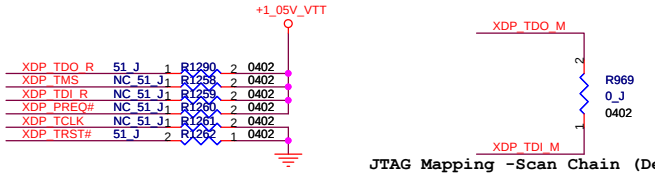
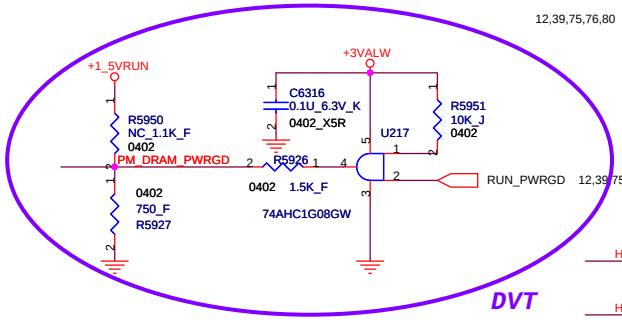
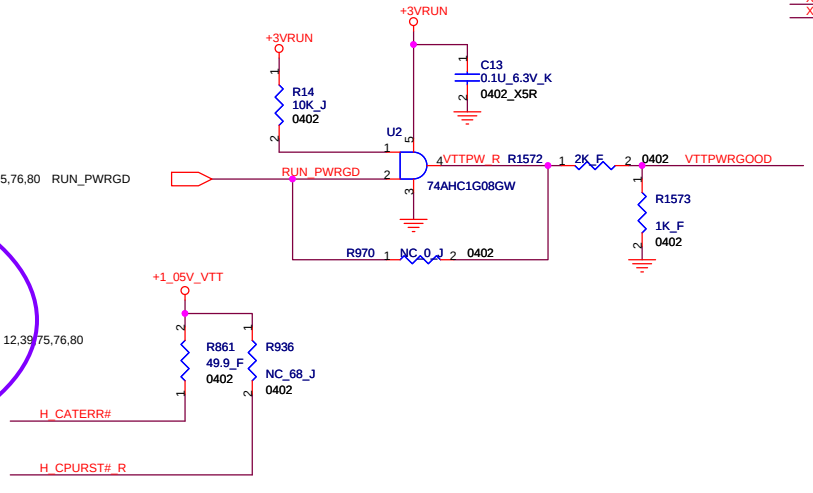
For Disable Arrandale Graphic
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on
Arrandale directly if motherboard only supports discrete graphics.



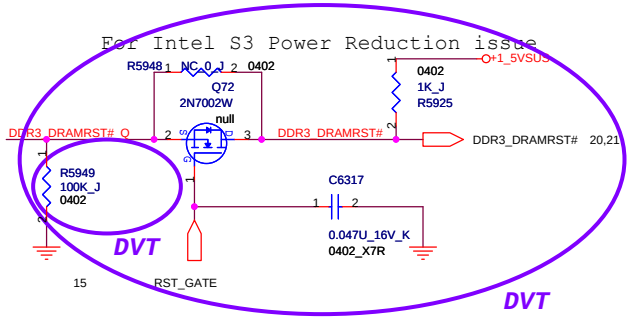
JTAG Mapping -Scan Chain (Default)

For Intel S3 Power Reduction issue

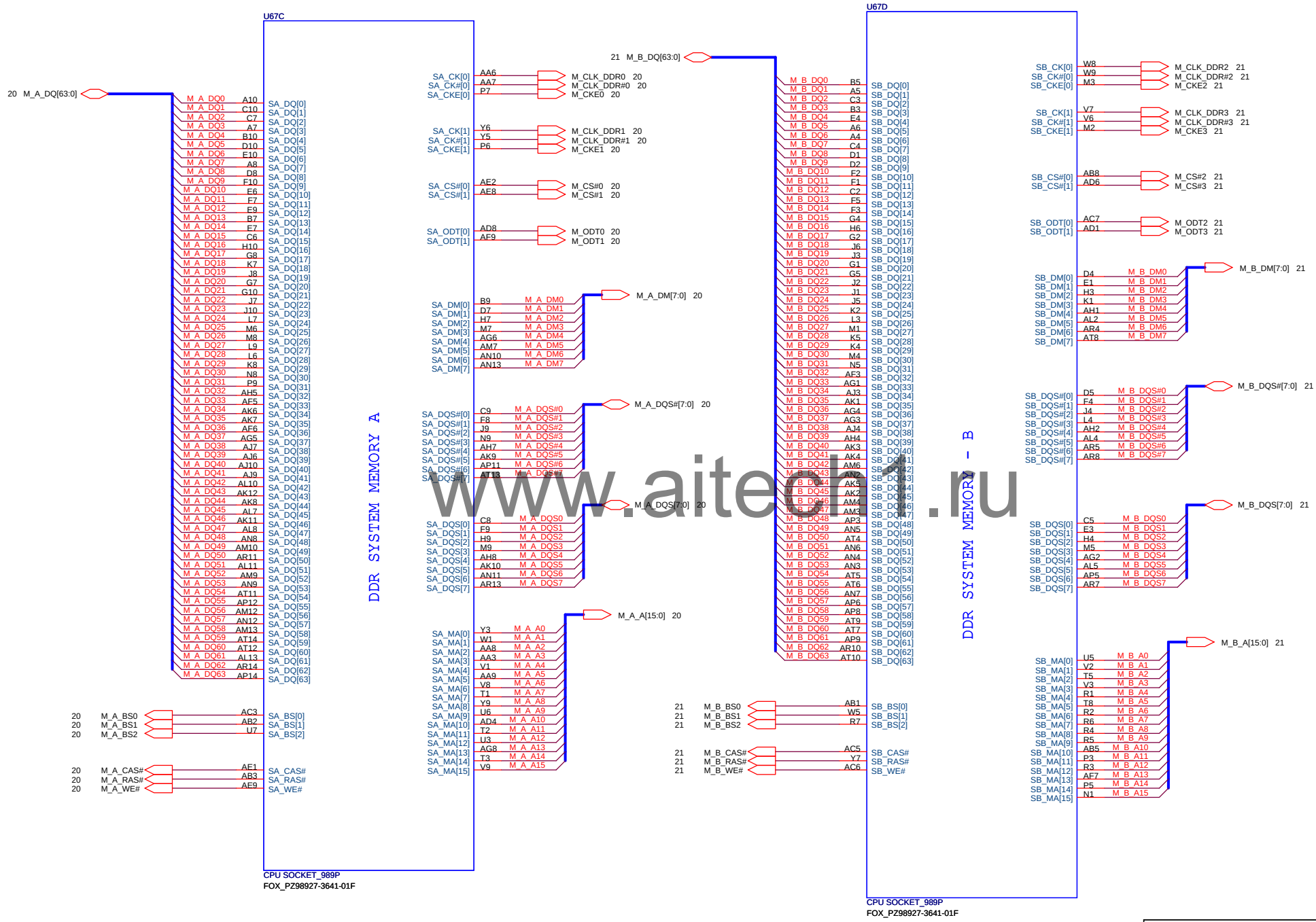




For Intel S3 Power Reduction issue



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (CLK,MISC,JTAG)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 4 of 86	



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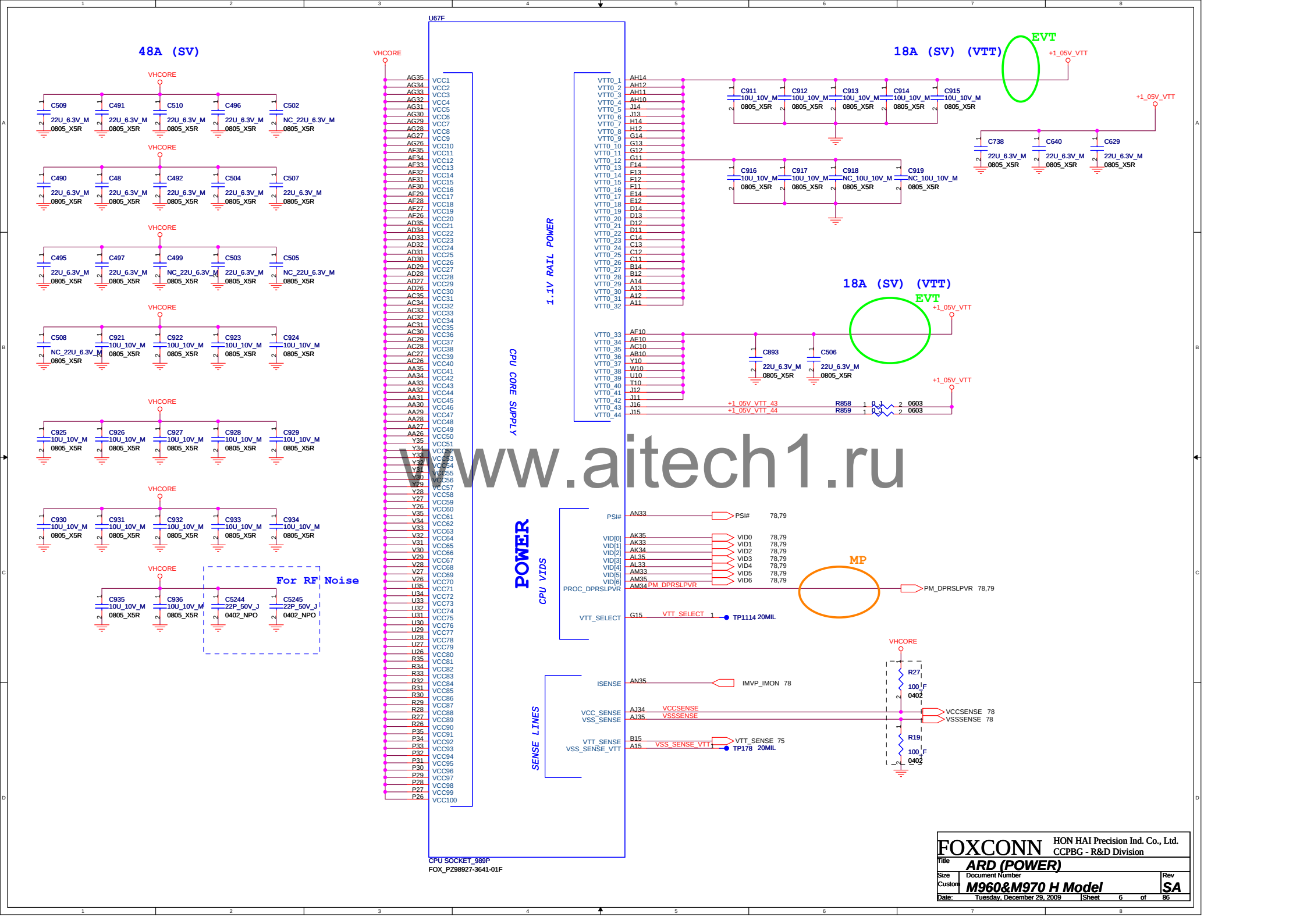
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (DDR3)		
Size A3	Document Number M960&M970 H Model		Rev SA
Date: Tuesday, December 29, 2009	Sheet 5 of 86		



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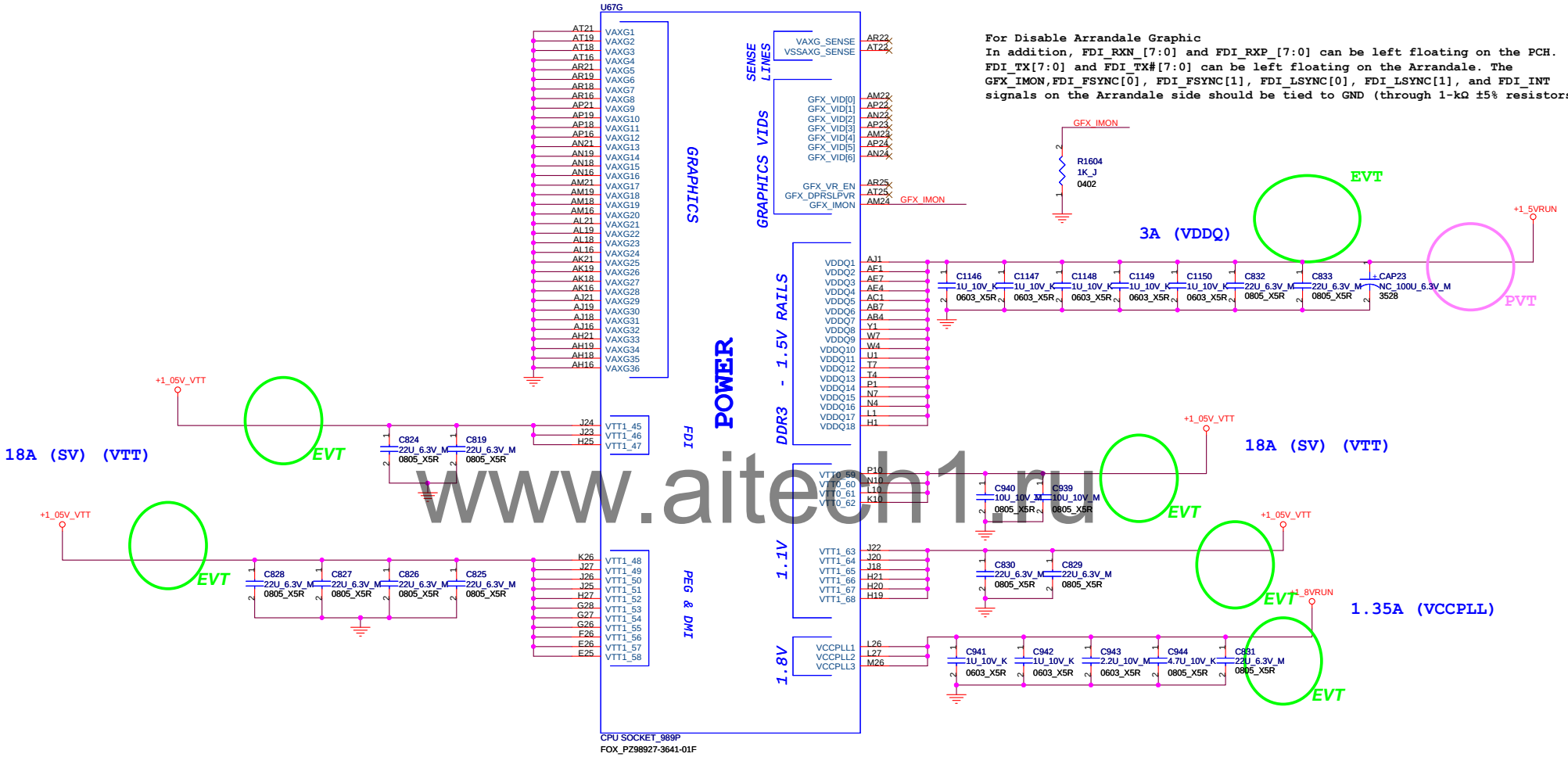
For Disable Arrandale Graphic
VAXG should be connected to GND when disable iGPU.

For Disable Arrandale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as no connect.

For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



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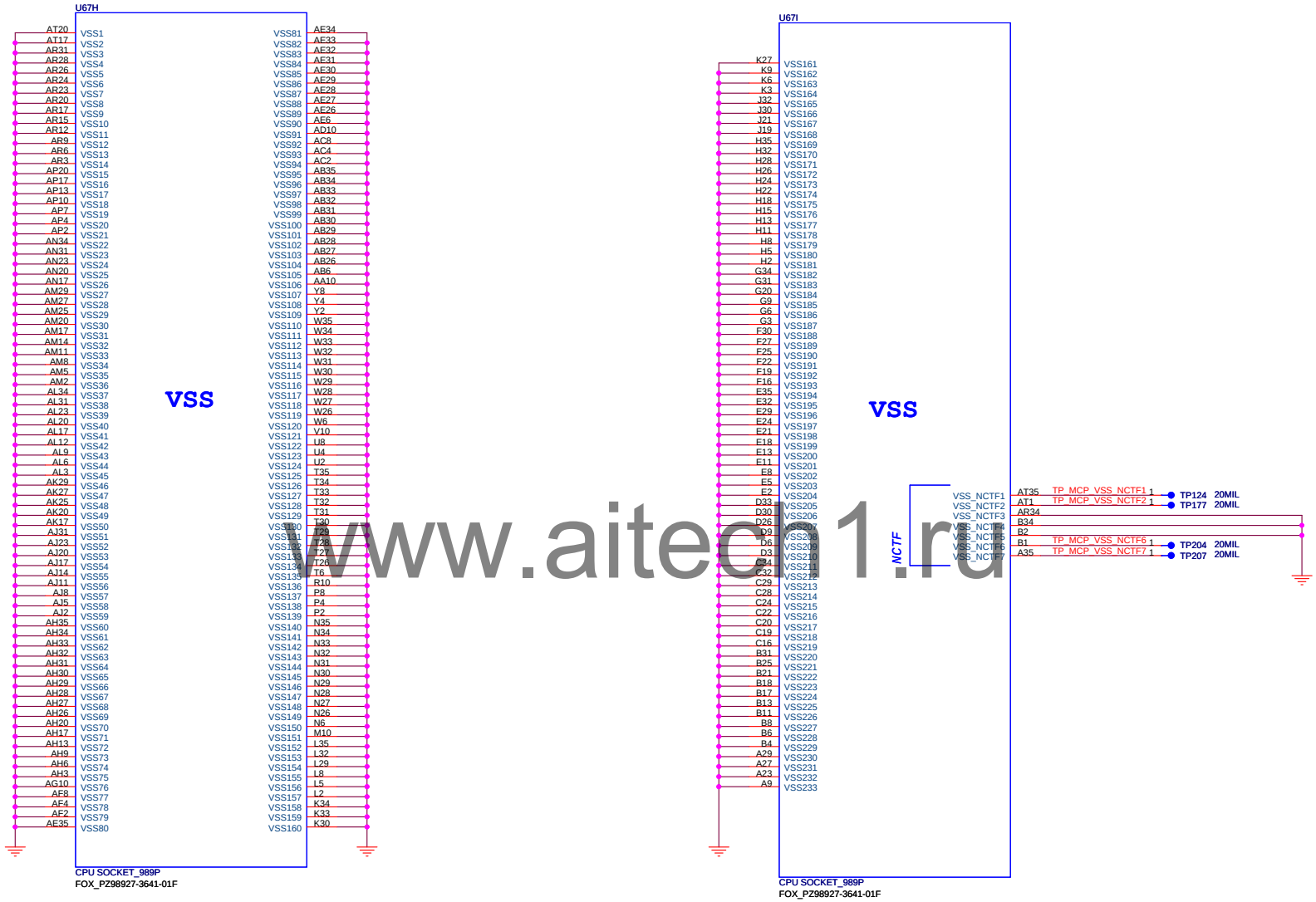
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (GRAPHICS POWER)	
Size Custom	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 7 of 86	



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FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (GND)	
Size Custom	Document Number M960&M970 H Model	Rev SA
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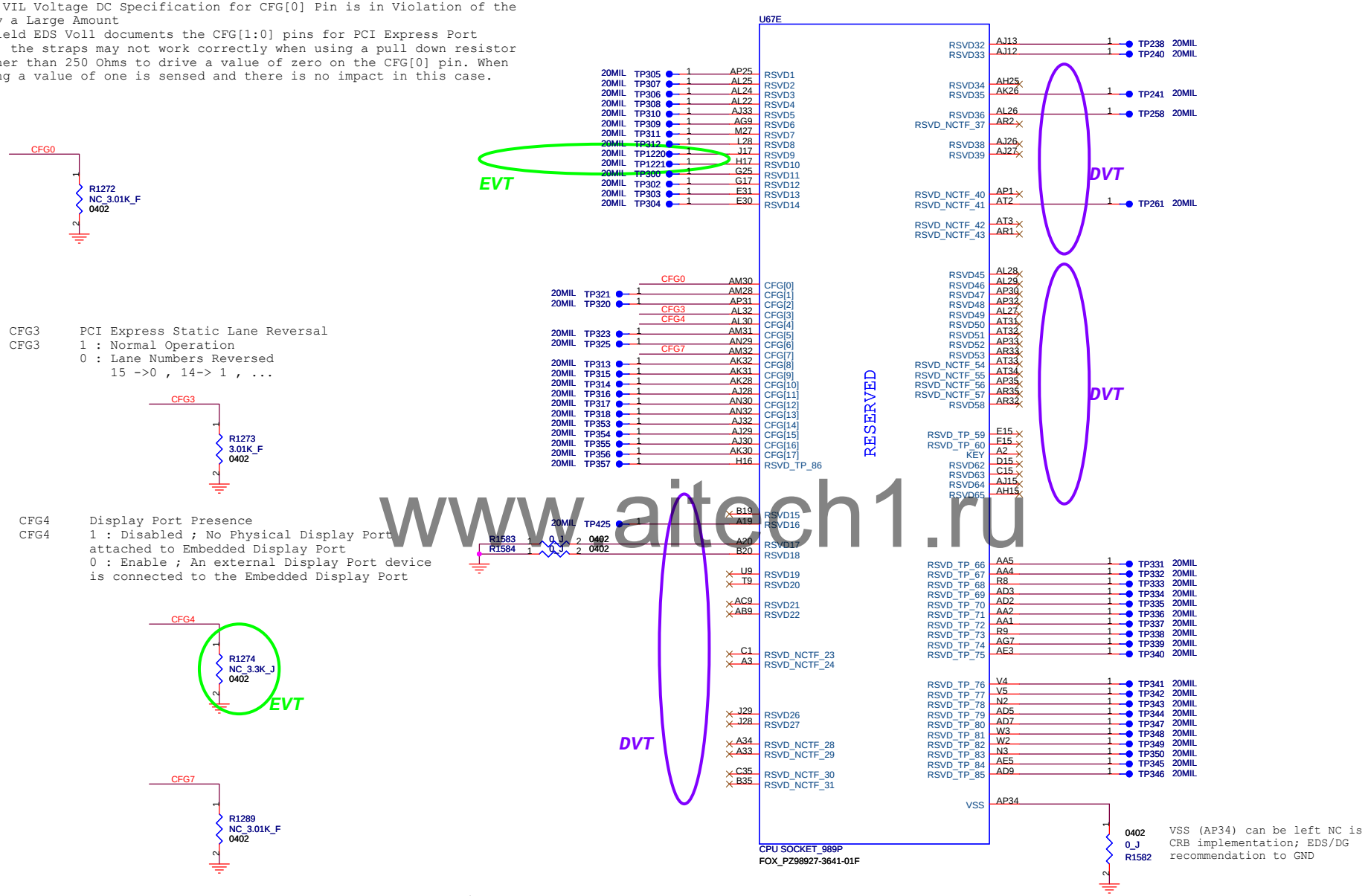
PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enable

3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.



CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 ->0 , 14-> 1 , ...

CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Port device is connected to the Embedded Display Port

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down).
Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.

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Title	ARD (RESERVED)	
Size A3	Document Number M960&M970 H Model	Rev SA
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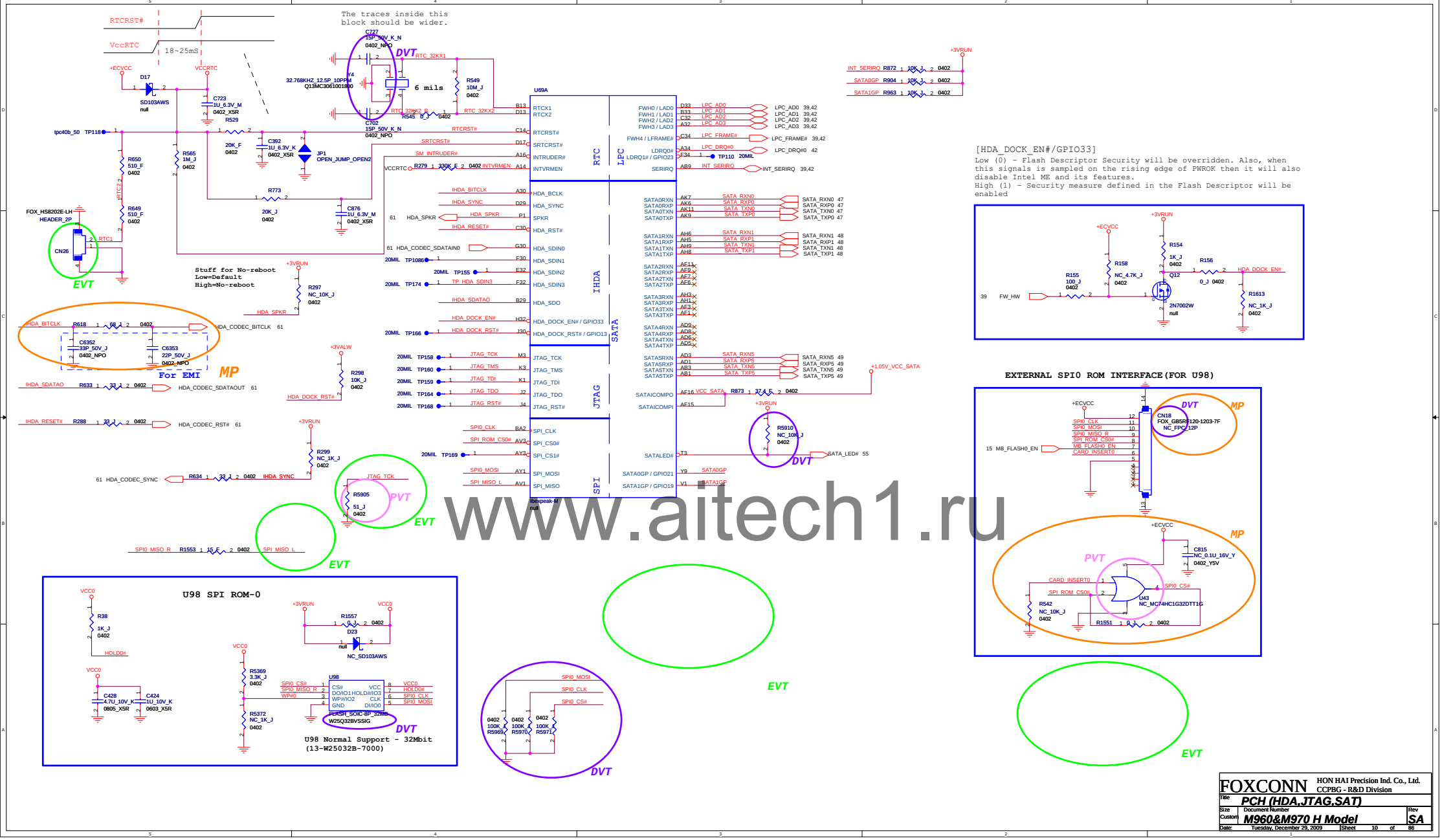

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: PCH (HDA,JTAG,SAT)

Size: Custom | Document Number: M960&M970 H Model | Rev: SA

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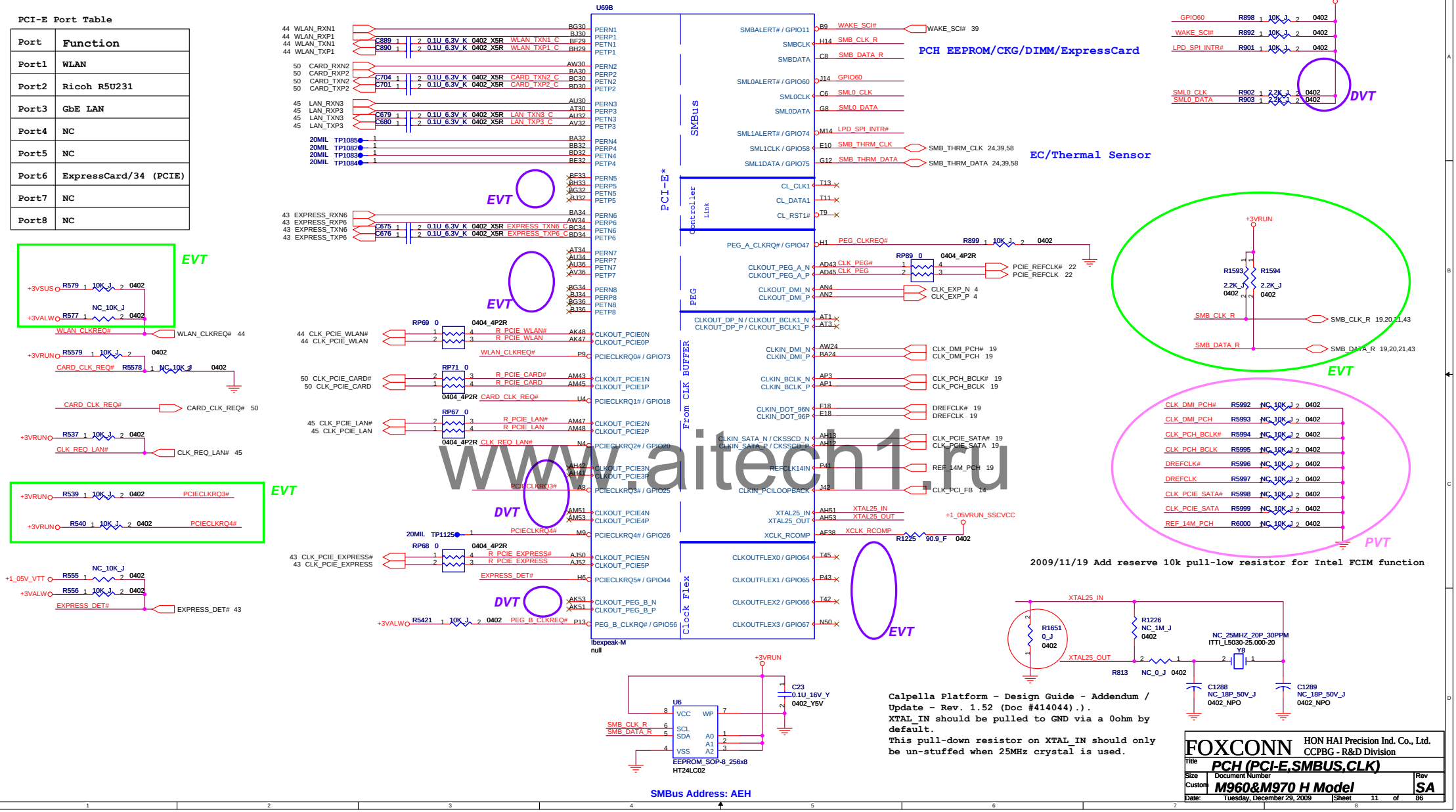
PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC



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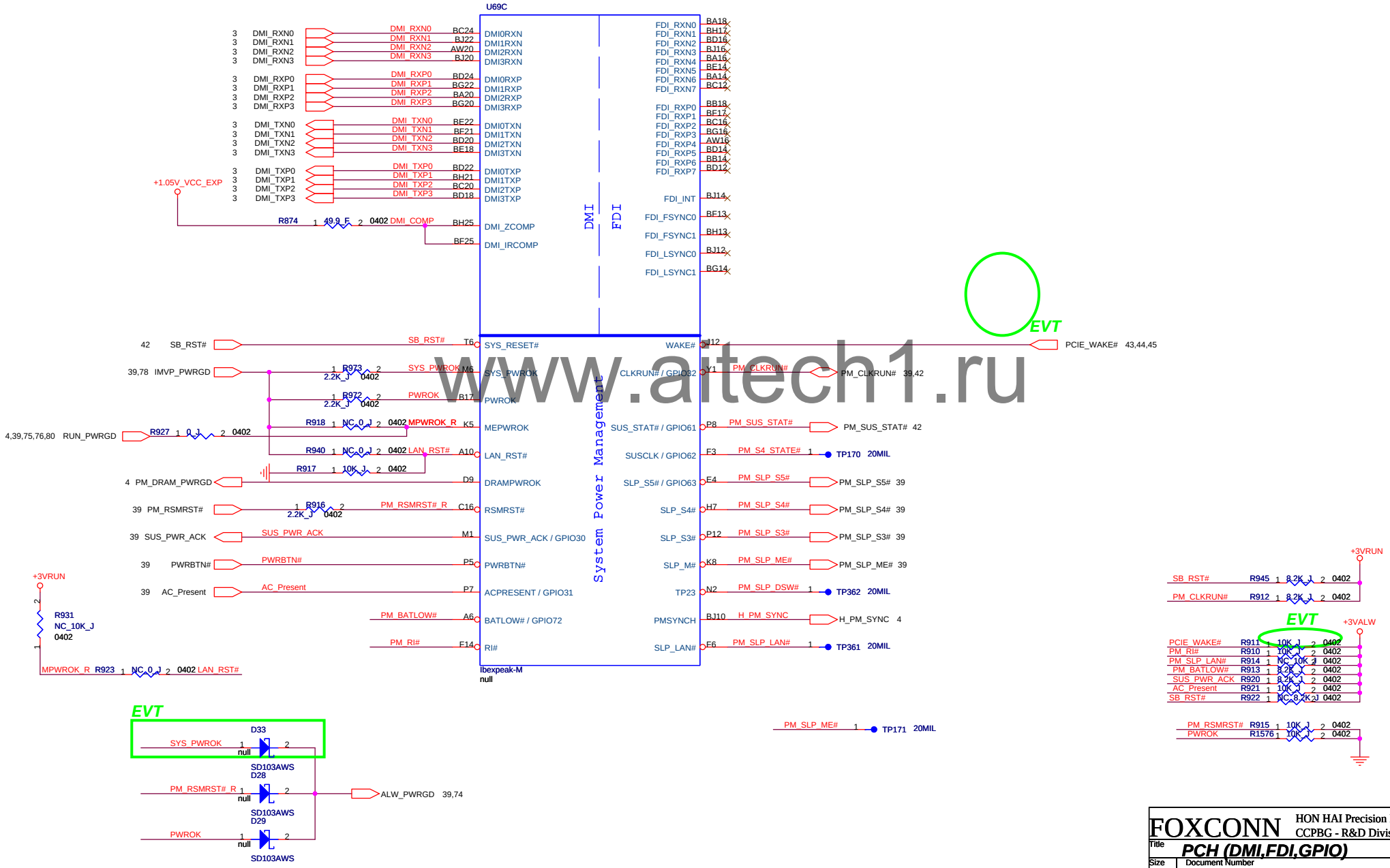
For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



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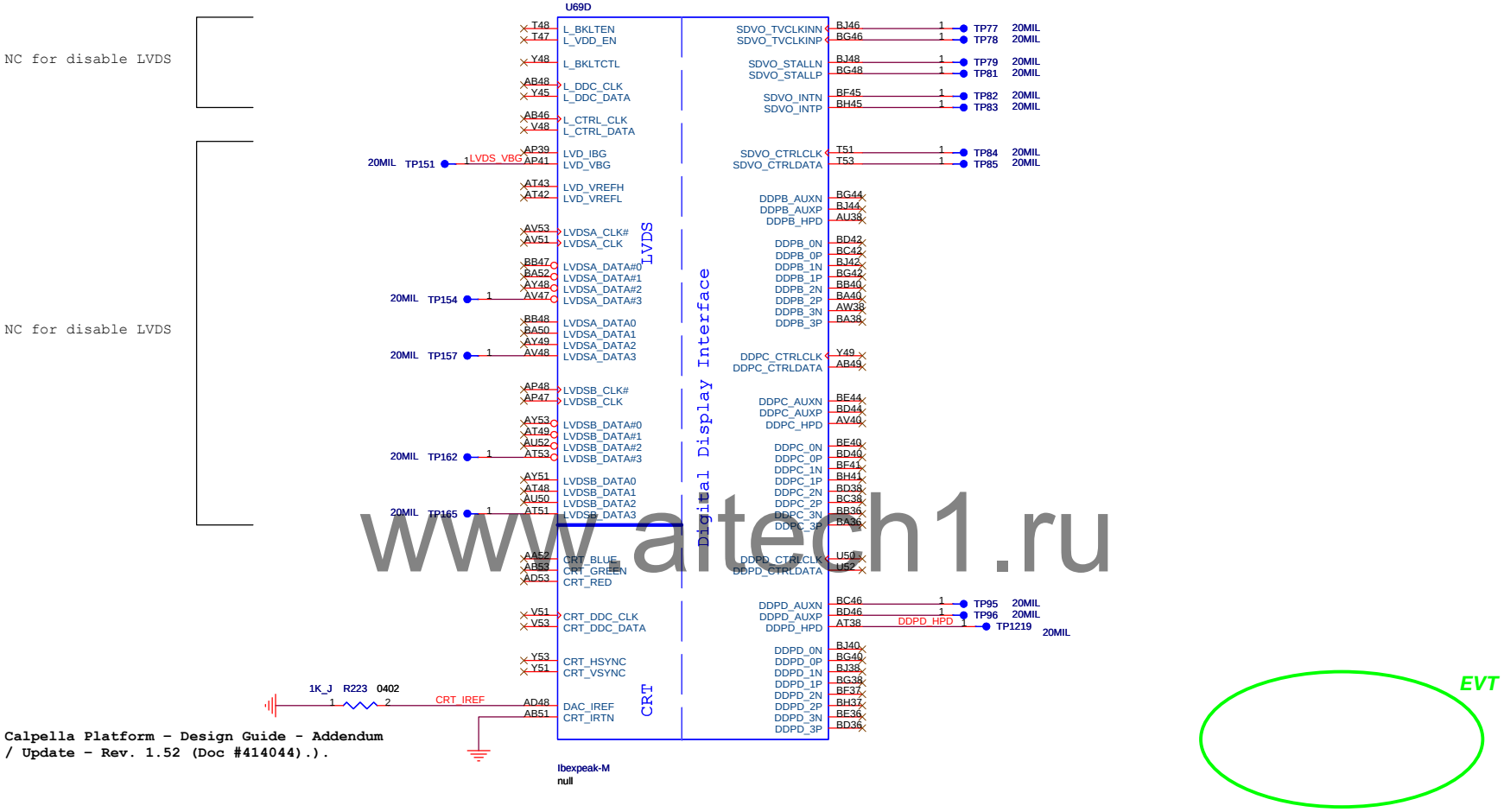
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (DMI,FDI,GPIO)		
Size A3	Document Number M960&M970 H Model		Rev SA
Date: Tuesday, December 29, 2009	Sheet 12 of 86		



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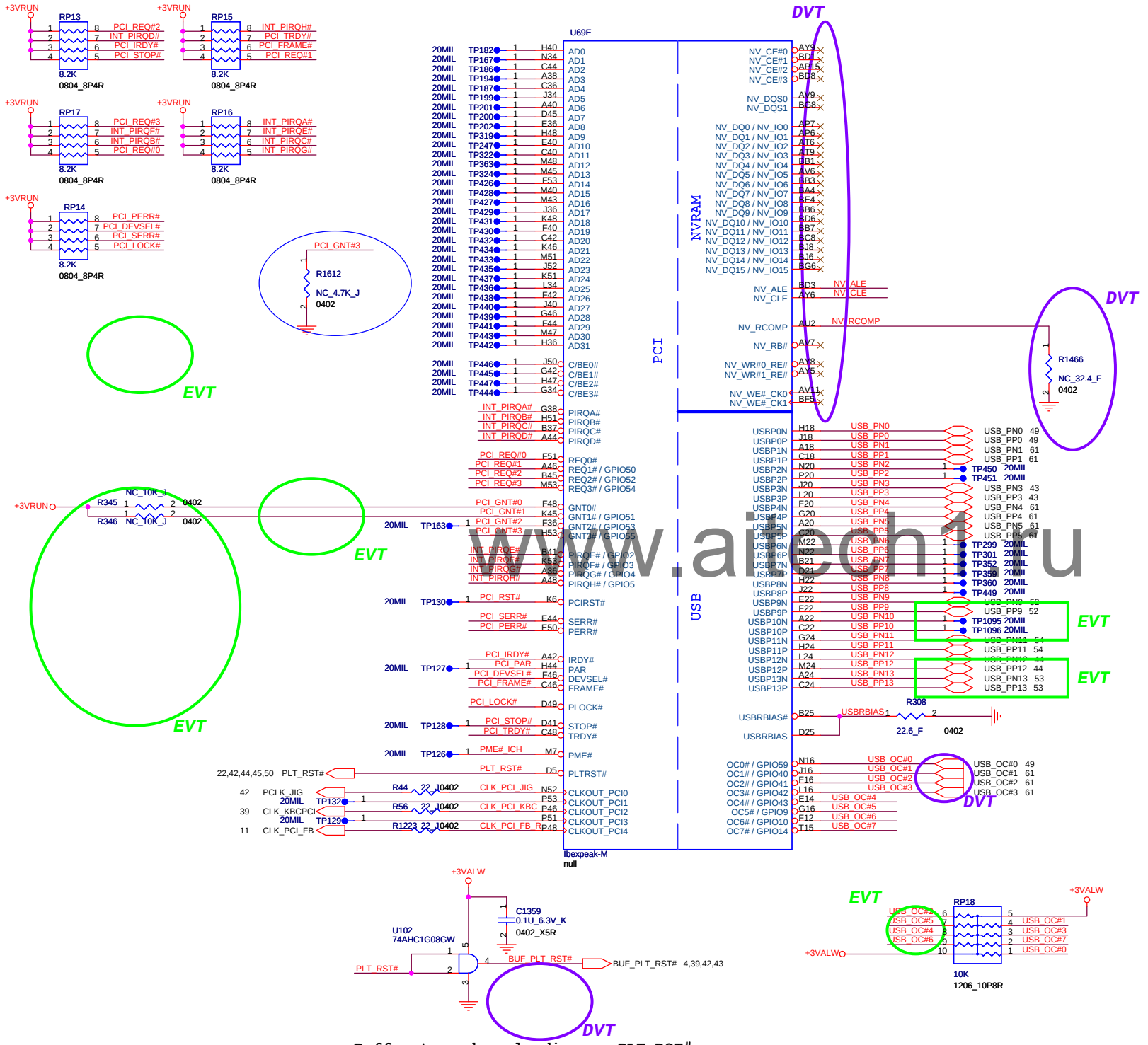
EVT

Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044).).

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (LVDS,DDI)	
Size: Custom	Document Number: M960&M970 H Model	Rev: SA
Date: Thursday, December 24, 2009	Sheet 13 of 86	



DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Danbury Technology
Disabled when Low
Enabled when High

USB PORT	Function
PORT-0	eSATA
PORT-1	External Port-2
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-3
PORT-5	External Port-1
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	
PORT-11	Felica
PORT-12	WLAN
PORT-13	Bluetooth

Buffer to reduce loading on PLT_RST#.

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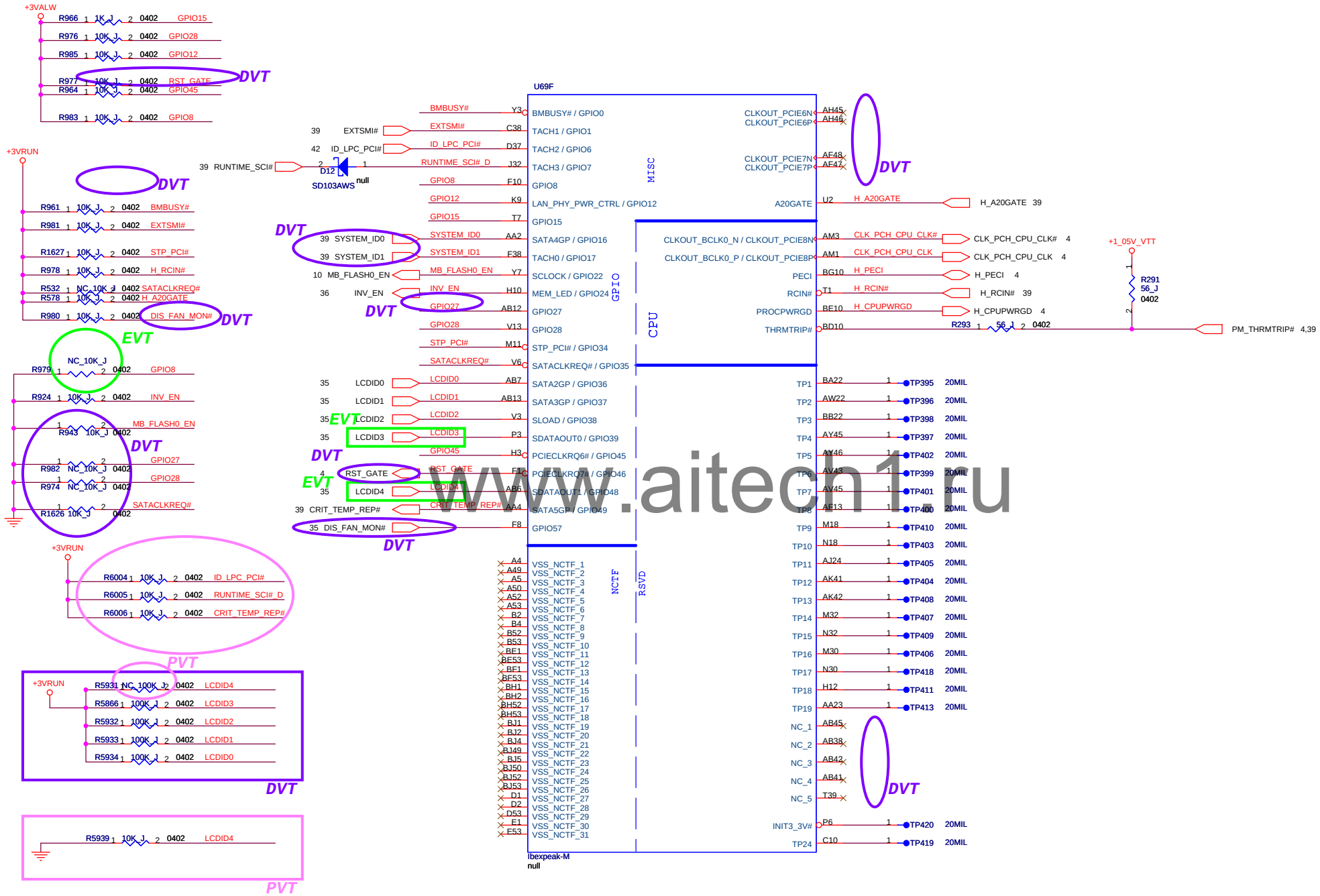
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: PCH (PCI,USB,NVRAM)

Size: A3 | Document Number: M960&M970 H Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 14 of 86



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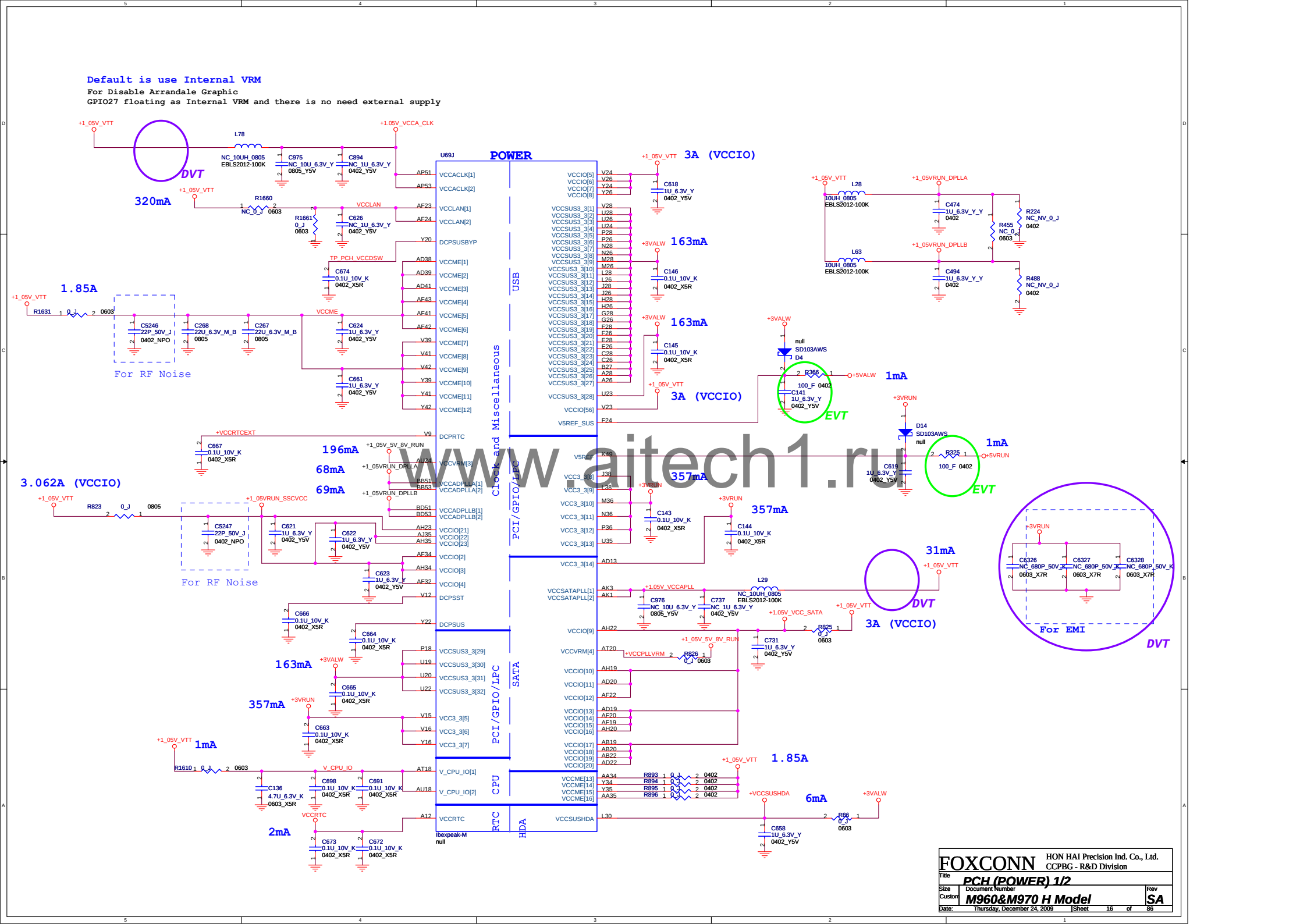
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (GPIO,VSS_NCTF,RSVD)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 15 of 86	


Default is use Internal VRM
For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply
POWER
U69J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
DVT
320mA
1.85A
For RF Noise
3.062A (VCCIO)
196mA
68mA
69mA
163mA
357mA
2mA
1mA
3A (VCCIO)
31mA
6mA
EVT
For EMI
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Title
PCH (POWER) 1/2
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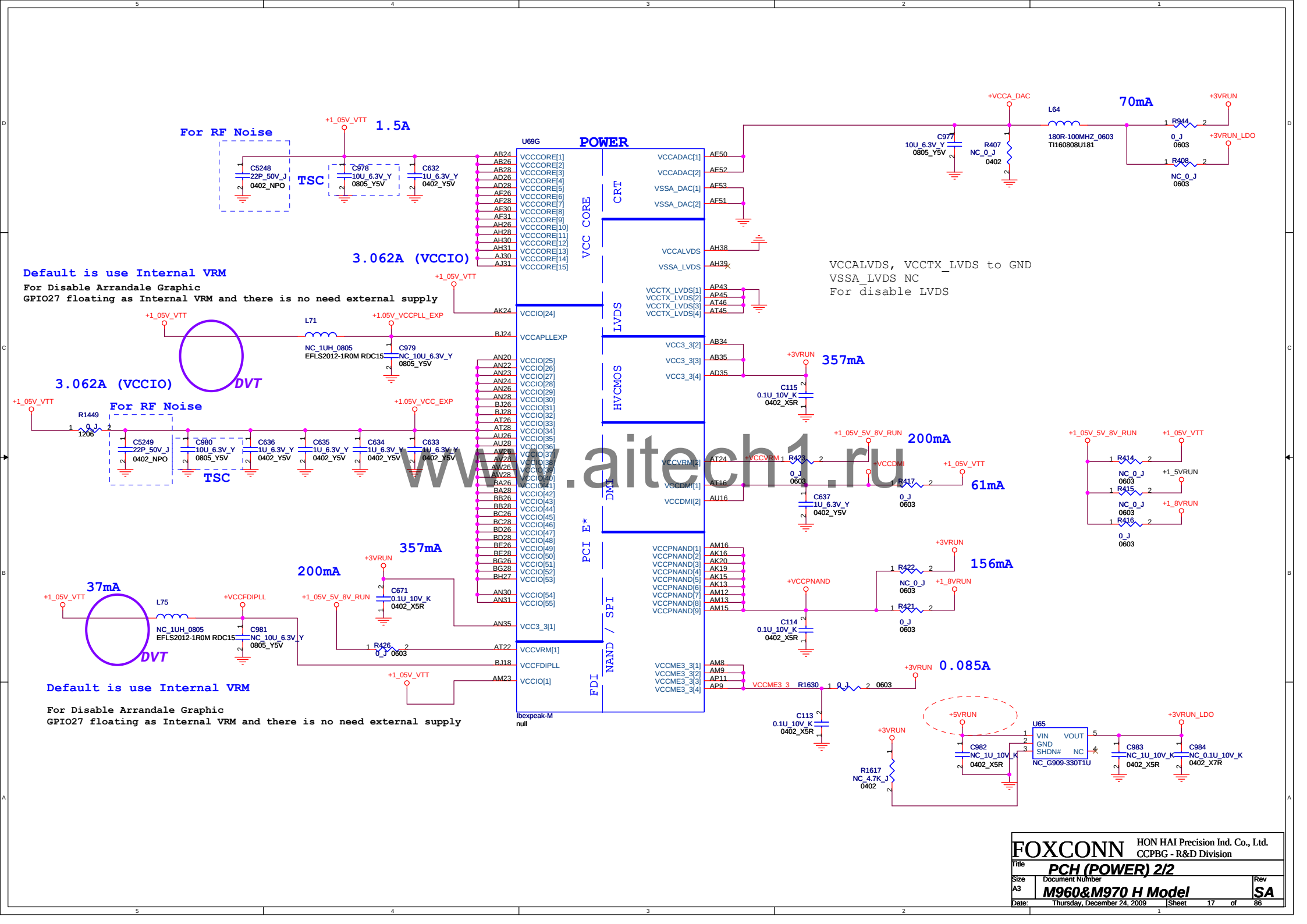

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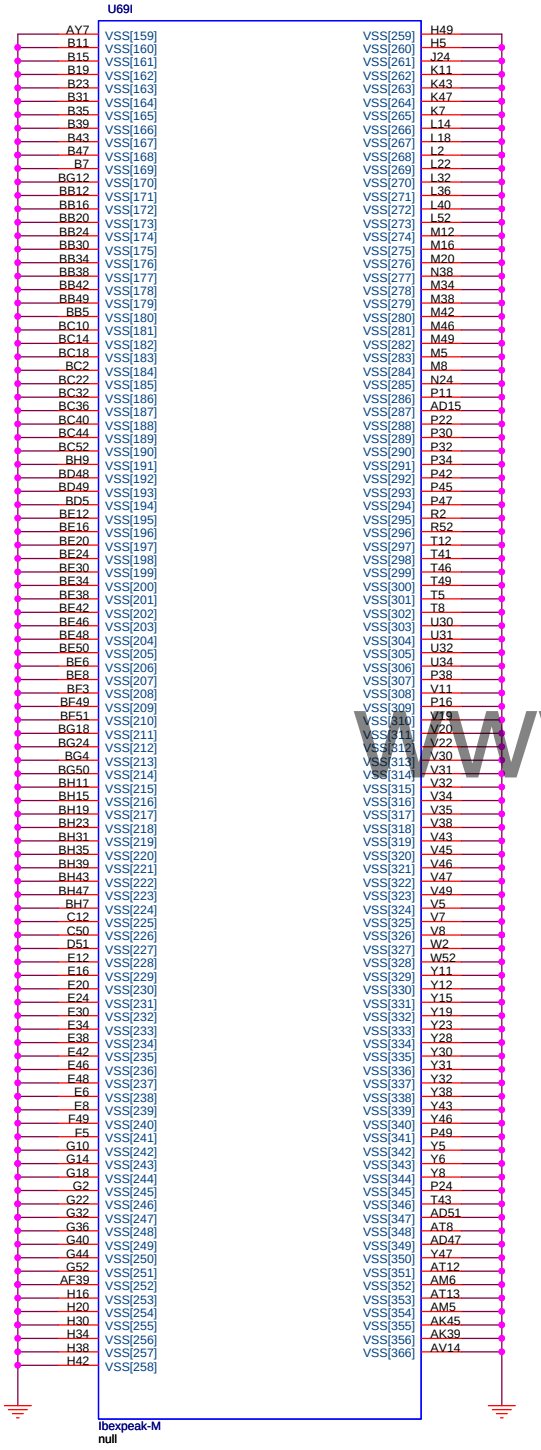
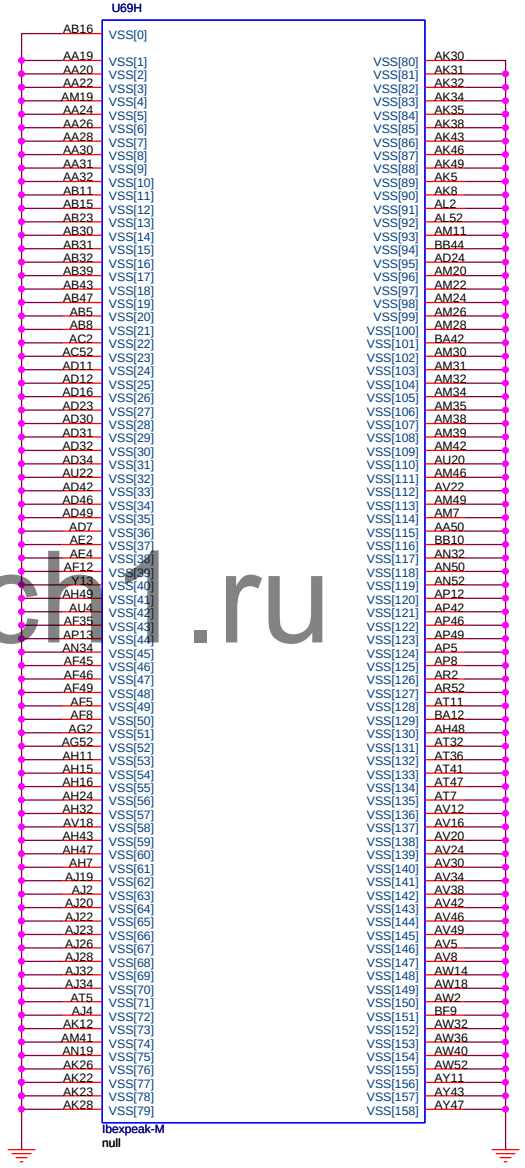
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 2/2	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 17 of 86	





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FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (VSS)	
Size A3	Document Number M960&M970 H Model	Rev SA
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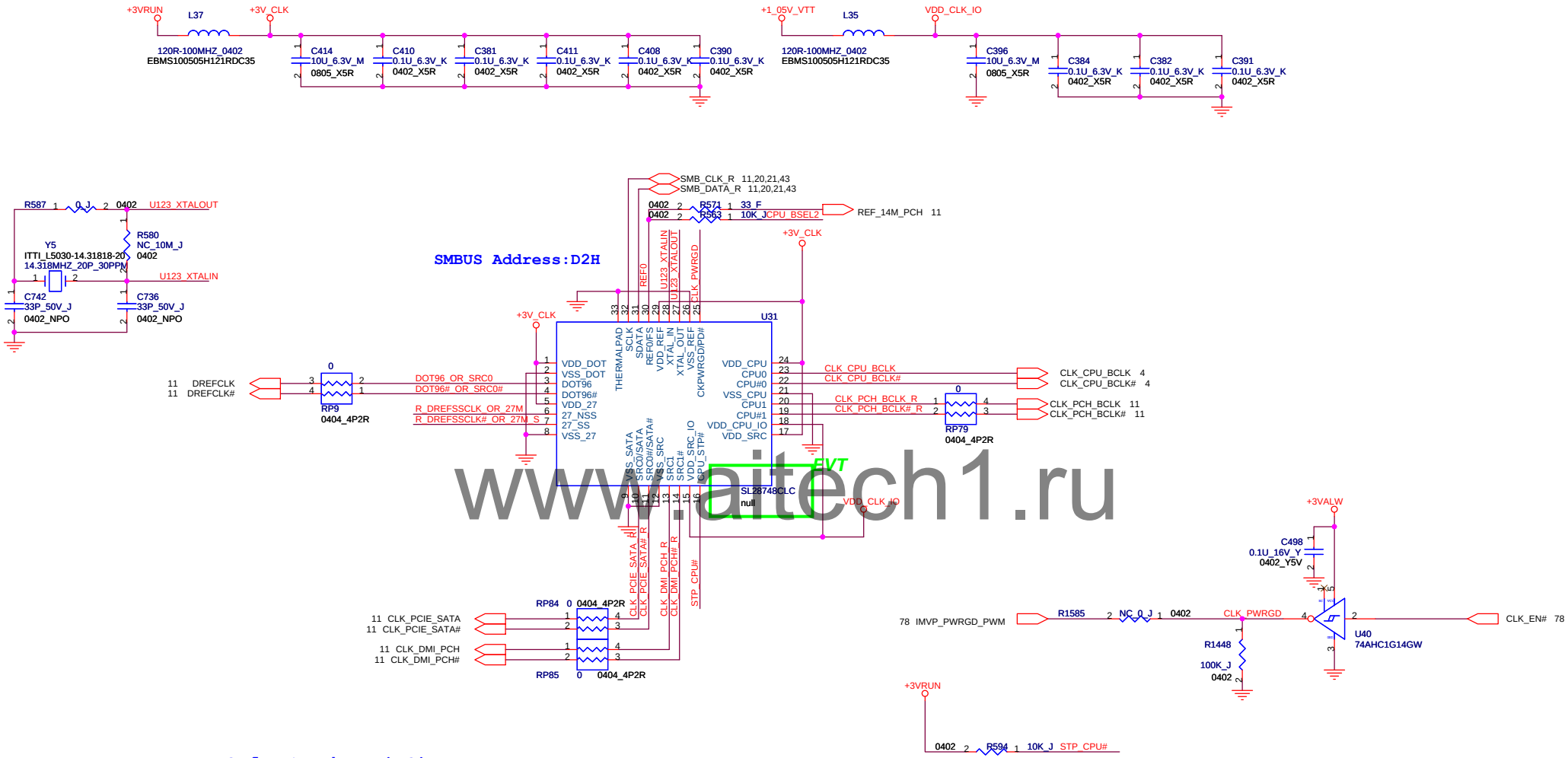

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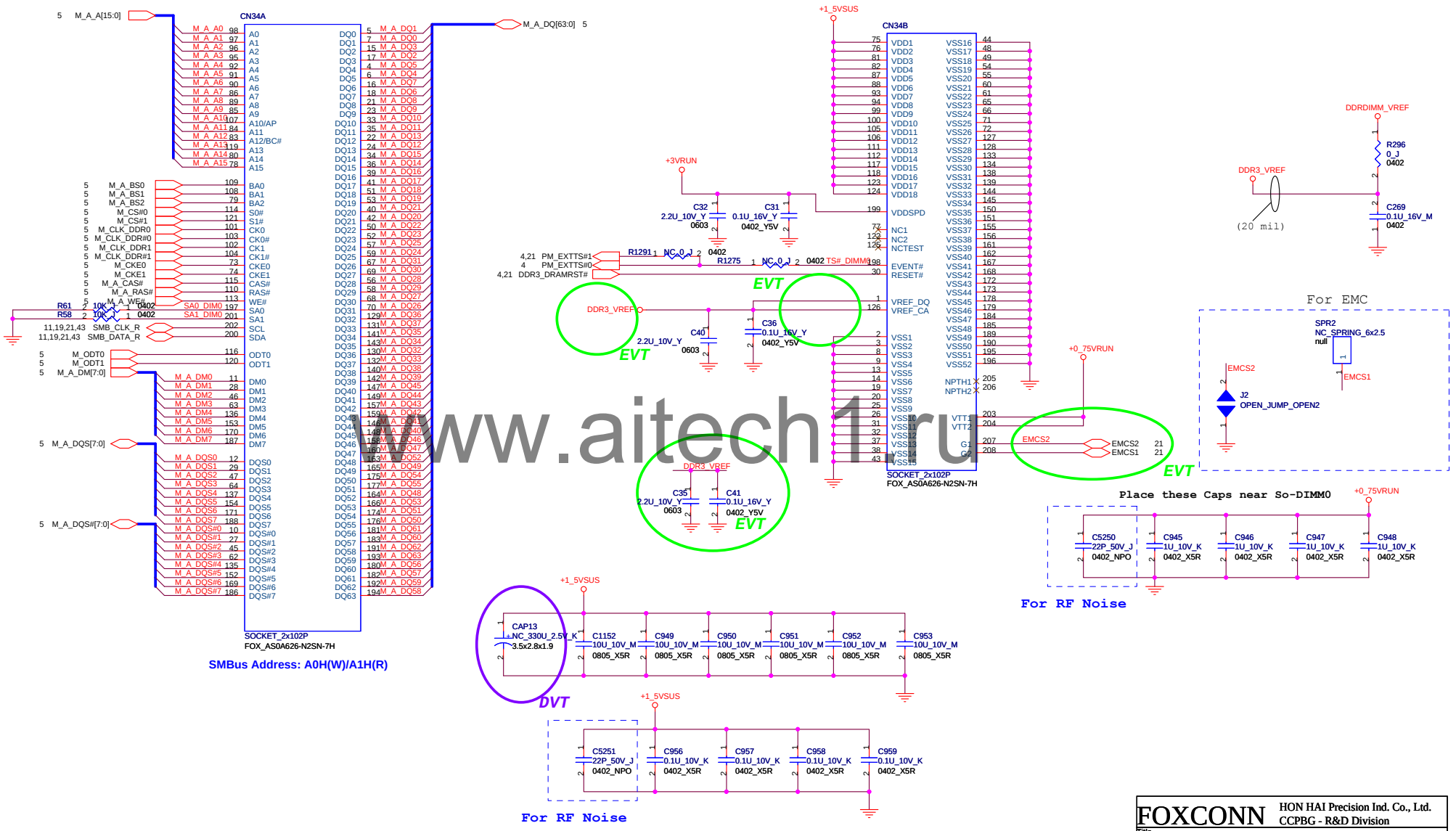
Frequency Select Pin (FS)

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

09/11/17 R_XTALSSIN be Connect a stable clock source (from clock gen SS 27MHz) to GPIO26_TCK.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CLOCK GEN		
Size A3	Document Number M960&M970 H Model		Rev SA
Date: Tuesday, December 29, 2009	Sheet 19 of 86		



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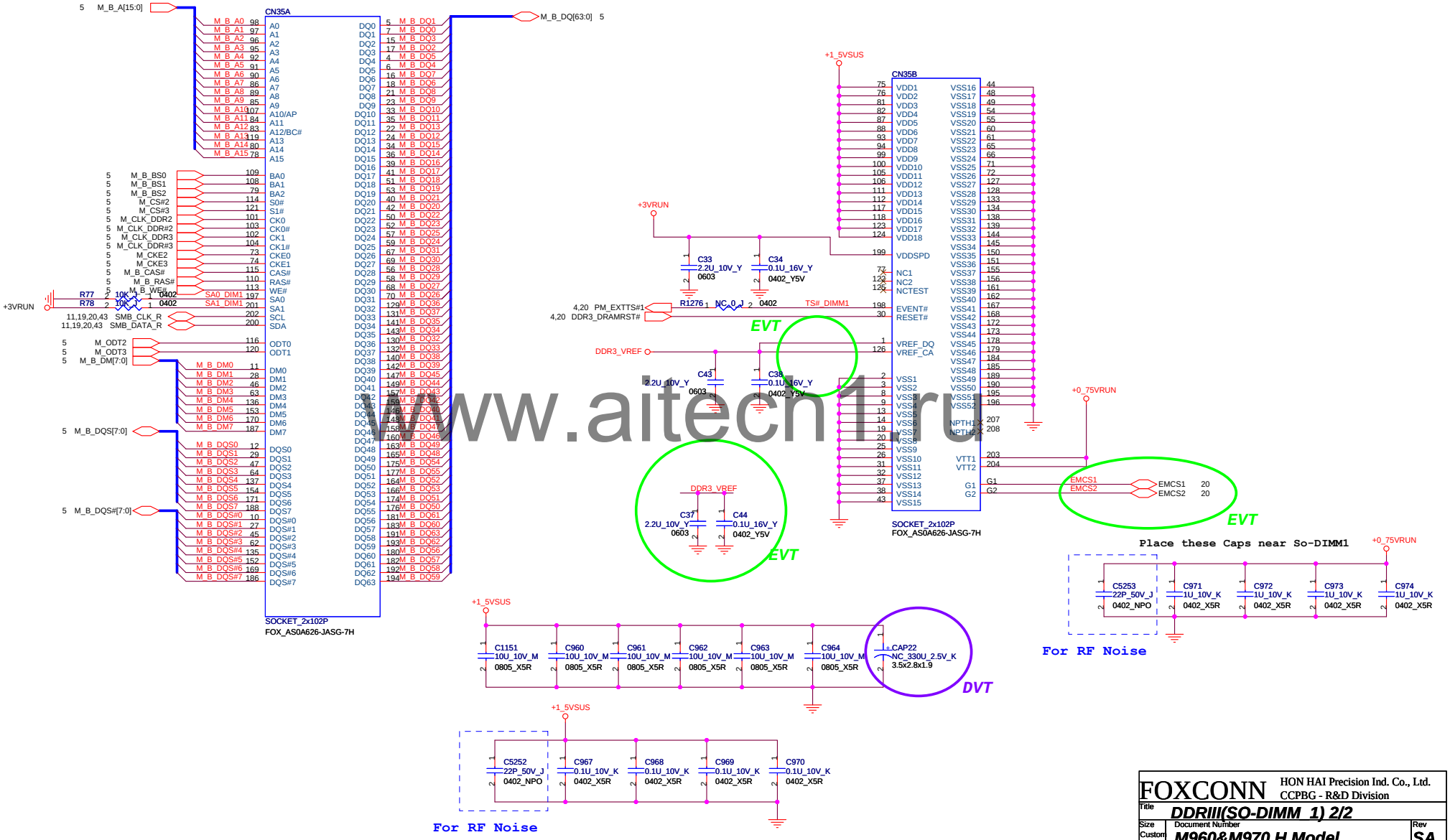
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDRIII(SO-DIMM_0) 1/2	
Size Custom	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 20 of 86	



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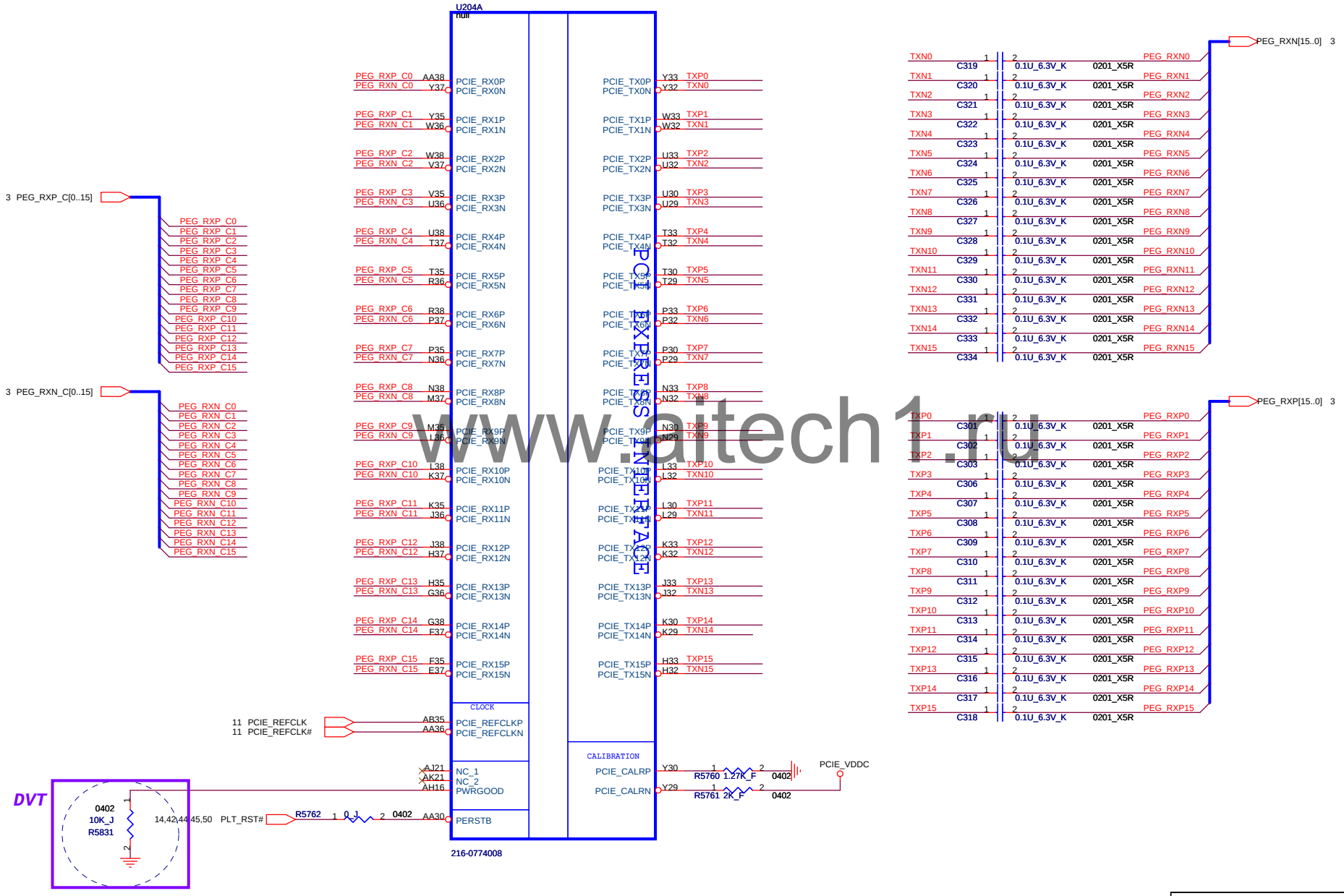
Title: DDRIII(SO-DIMM 1) 2/2

Size: Custom | Document Number: M960&M970 H Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 21 of 86



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Ball AH16:
For M96 this pin NC.
For Madison-M2 and Park-M2
the PWRGOOD ball must be connected to ground.
For M97-M2 PWRGOOD input must be provided externally.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	VGA (PCI-E) 1/6		
Size A3	Document Number M960&M970 H Model		Rev SA
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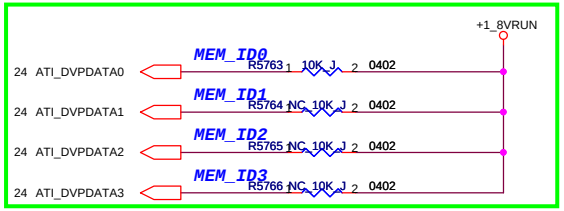
EVT

Strap for DDR3 VRAM
ATI_DVPDATA[3 : 0]

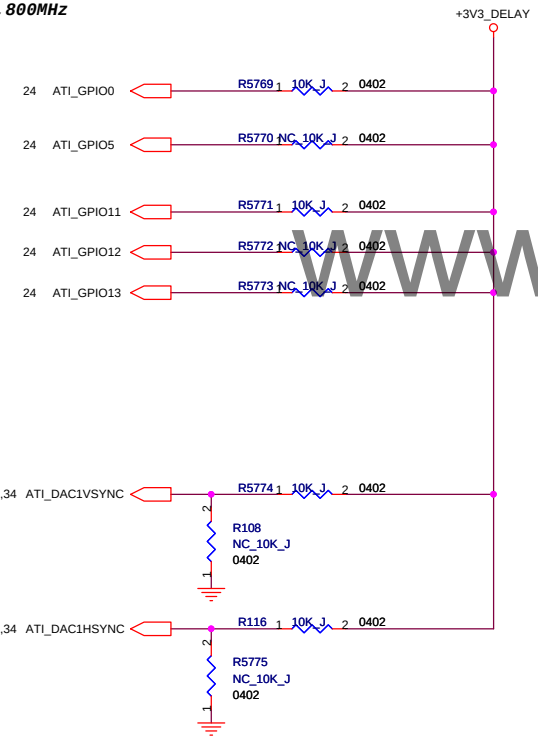
EVT




```
For M960/M970 M92-M2 XTX / Park-XT
0001 64Mx16  Reserve   x4pcs
0010 64Mx16  Hynix *   x4pcs
0011 64Mx16  Samsung** x4pcs
0101 64Mx16  Reserve   x4pcs
0110 64Mx16  Elpida*** x4pcs
0111 64Mx16  AMD****   x4pcs

For M960/M970 Madsion-LP
0001 64Mx16  Reserve   x8pcs
0010 64Mx16  Hynix *   x8pcs
0011 64Mx16  Samsung** x8pcs
0101 64Mx16  Reserve   x8pcs
0110 64Mx16  Elpida*** x8pcs
0111 64Mx16  AMD****   x8pcs
P.S. * means Hynix H5TQ1G63BFR-12C,800MHz
     **means Samsung K4W1G1646E-HC12T00,800MHz
     ***means Elpida EDJ1116DBSE-DJ-F,1333MHz
     ****means AMD 23EY2387MA-12,800MHz
```

```
If no ROM attached, GPIO[13:12:11]
CONFIG{2:0}
controls the memory aperture size.
64MB                 010
128MB                000
256MB                001
512MB                001
```




```
1   Enable HD Audio
0   Disable HD Audio

1   Enable HDMI
0   Disable HDMI
```

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN name	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	
AC_BATT	GPIO_5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
PWRCNTL_0 PWRCNTL_1	GPIO_6 GPIO_15 GPIO_20	Power Control signals control the core voltage regulator. At Reset, these signals will be inputs with weak internal pull-down resistors. VBIOS can define these signals to be either 3.3-V outputs or open drain outputs. The output state (high/low) of these signals is programmable for each PowerPlay state.	
BB_EN	GPIO_21	Back Bias (BB) control: When GPIO_21_BB_EN = 0 V, then back bias is disabled on the PCB (i.e. BPP = VDDC). When GPIO_21_BB_EN = 3.3 V, then back bias is enabled on the PCB (i.e. BPP = VDDC +Offset). Can function as a GPIO if not required for BB control.	
BLON	GPIO_7	Controls Backlight On/Off. Active high. If not needed as the backlight enable signal, it can alternatively be used as a GPIO or an open drain type output. Note: External pull-down recommended	
VGA_DIS	GPIO_9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	
CONFIG[0] CONFIG[1] CONFIG[2]	GPIO_11 GPIO_12 GPIO_13	If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	
BIOS_ROM_EN	GPIO_22	Enable external BIOS ROM device 0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	
SSIN	GPIO_16	Spread Spectrum clock input for memory clock and/or engine clock (maximum down spread of -2.5%). Requires a spread version of 27 MHz(The modulation rate is 30-50 KHz.)	
THERMAL_INT	GPIO_17	Thermal monitor interrupt Can be set as either: 1) An input from an external temperature sensor (ALERTb) , or 2) An output signaling that the ASIC temp (measured by the internal sensor) is above the high threshold or below the low threshold.Output can be open drain or 3.3-V output.(active low by default)	
CLKREQB	GPIO_23	Reserve	

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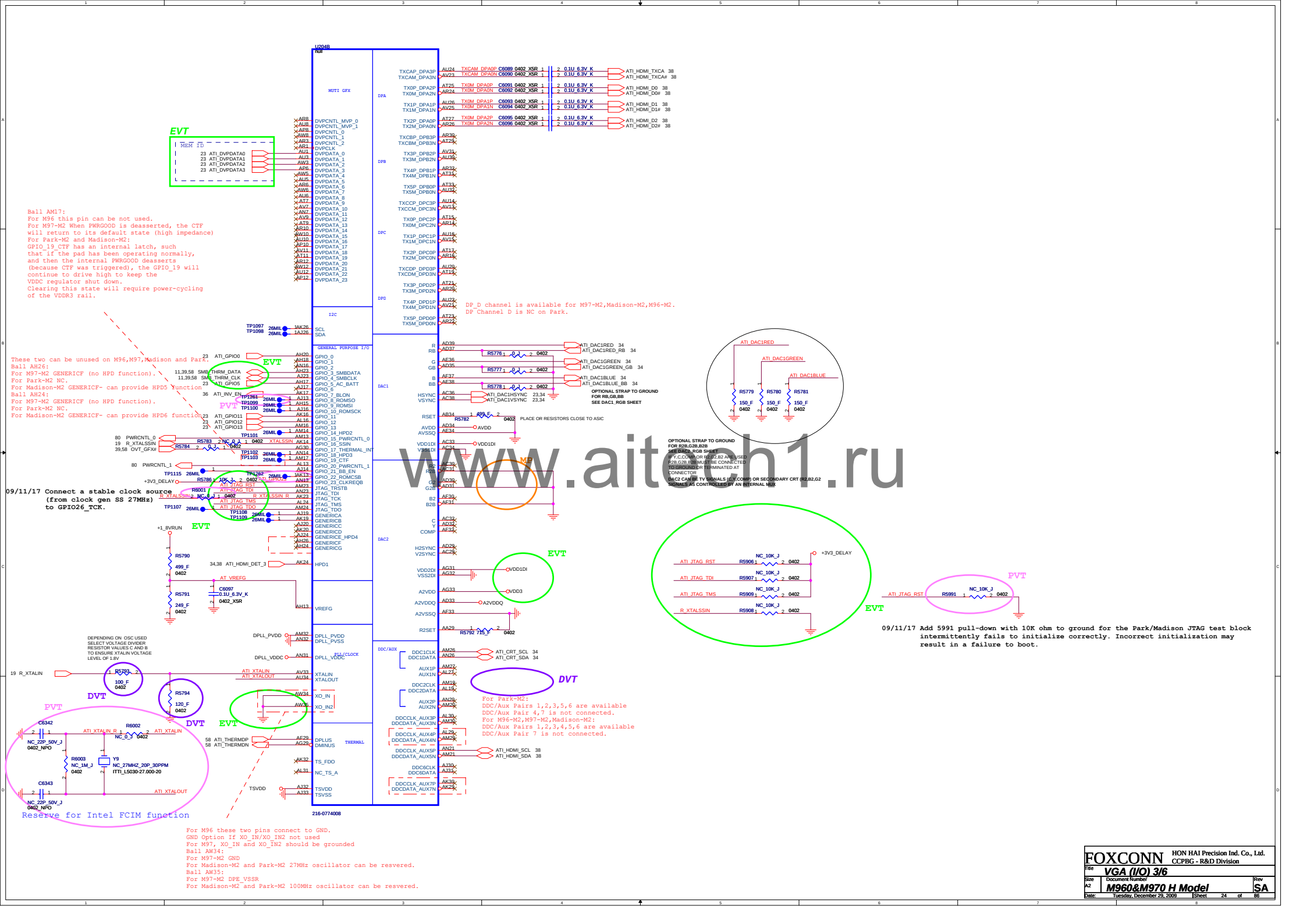

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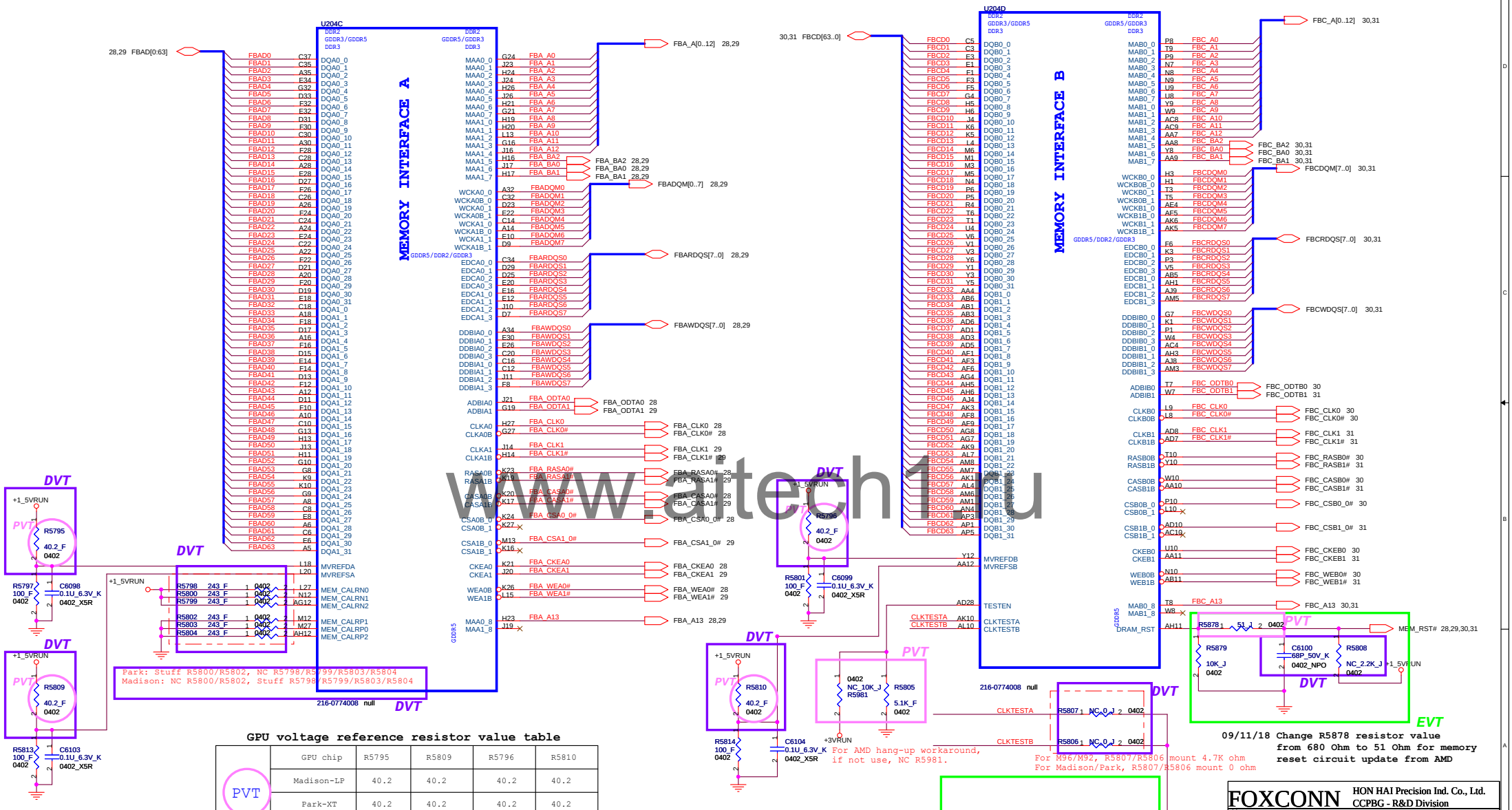

GPU voltage reference resistor value table

	GPU chip	R5795	R5809	R5796	R5810
PVT	Madison-LP	40.2	40.2	40.2	40.2
	Park-XT	40.2	40.2	40.2	40.2
	M92 XTX	100	100	100	100

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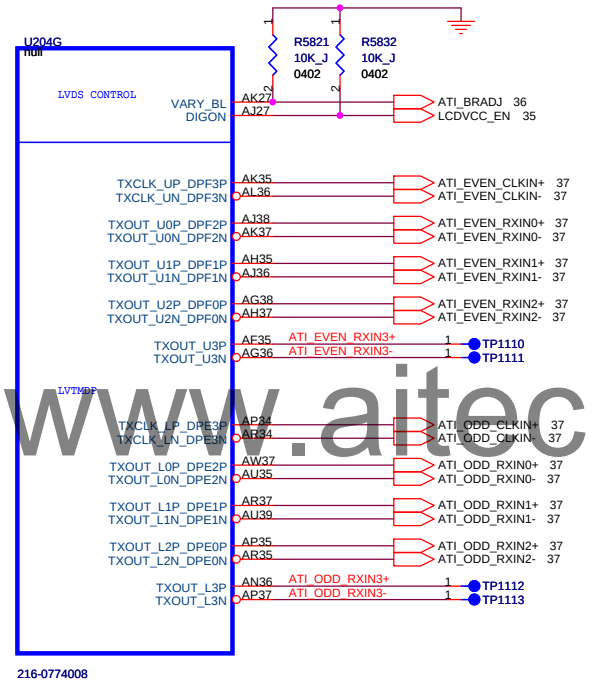

TXCLK =U=EVEN
TXOUT=U=EVEN
TXCLK =L=ODD
TXOUT=L=ODD

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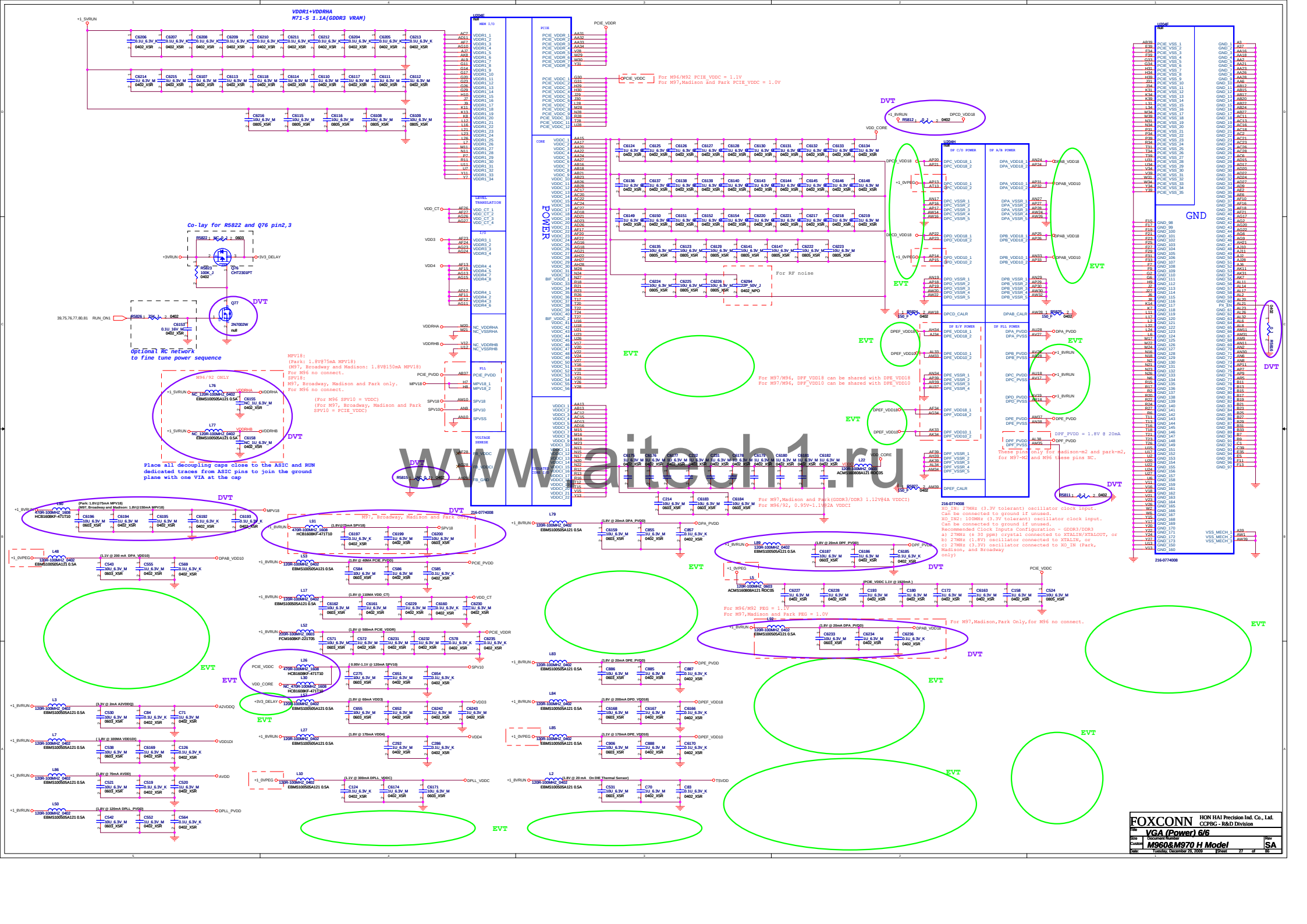
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA (LVDS) 5/6	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 26 of 86	



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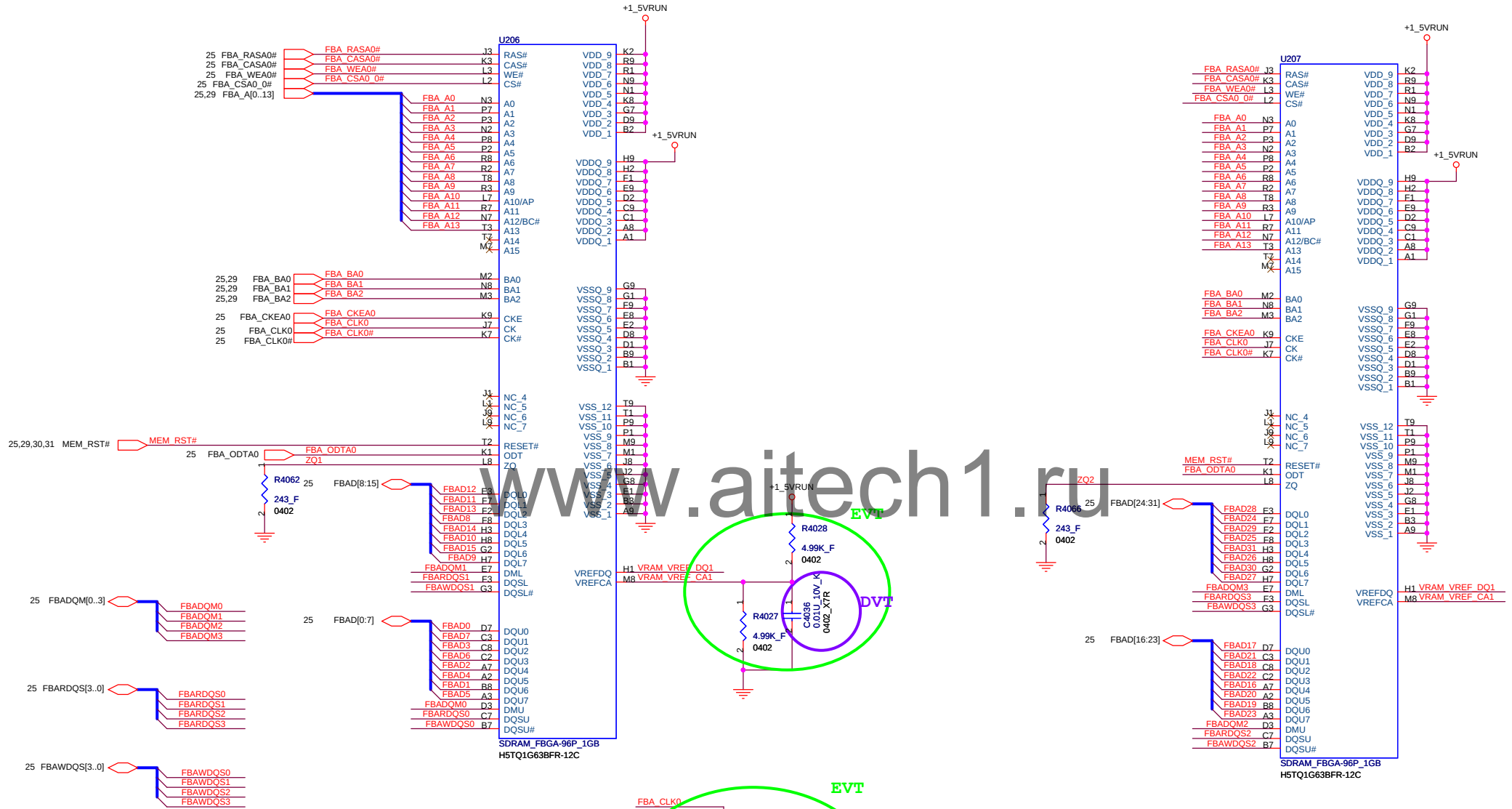

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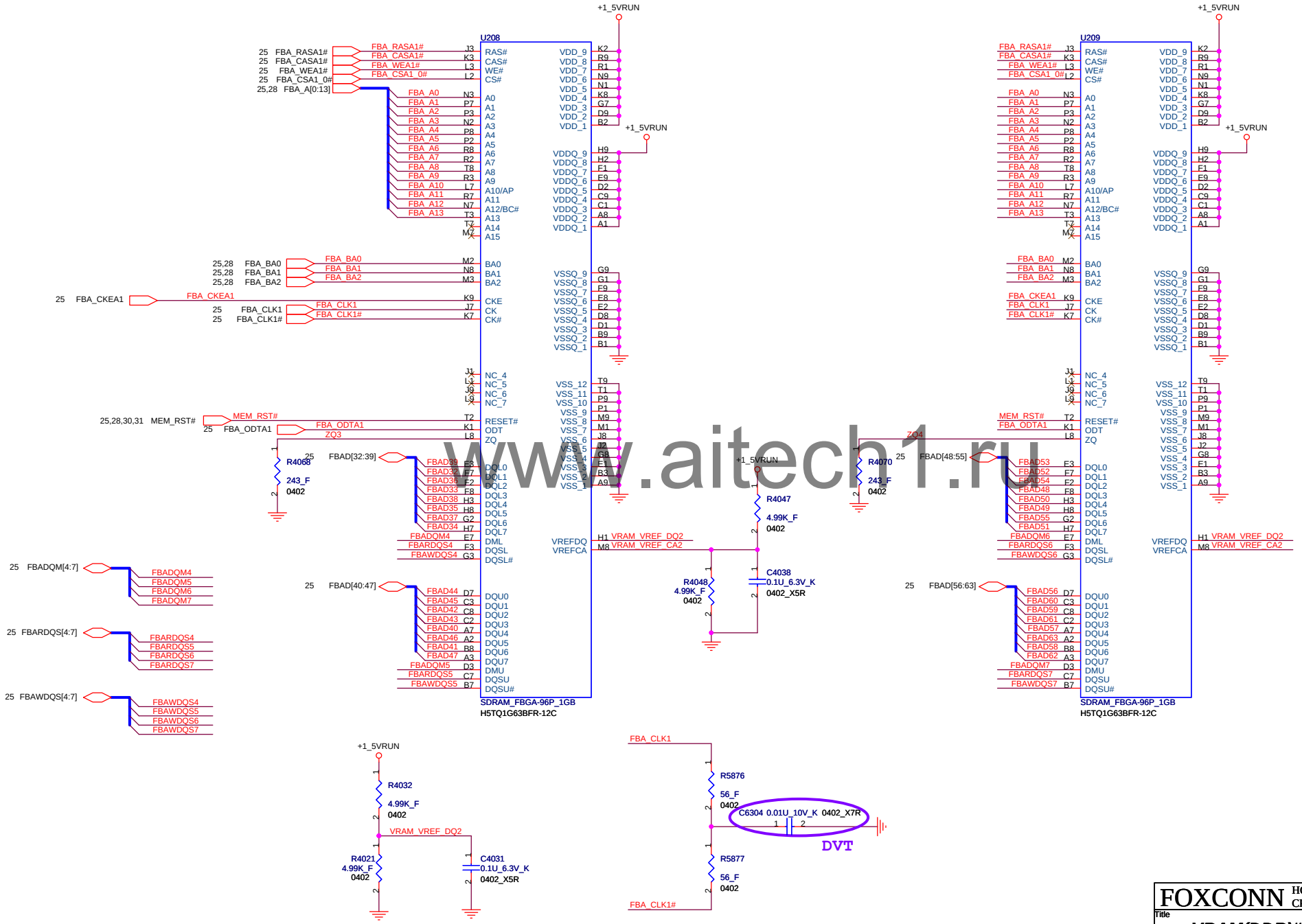
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM(DDR)# 1/4
Size A3	Document Number M960&M970 H Model
Rev	SA
Date: Tuesday, December 29, 2009	Sheet 28 of 86



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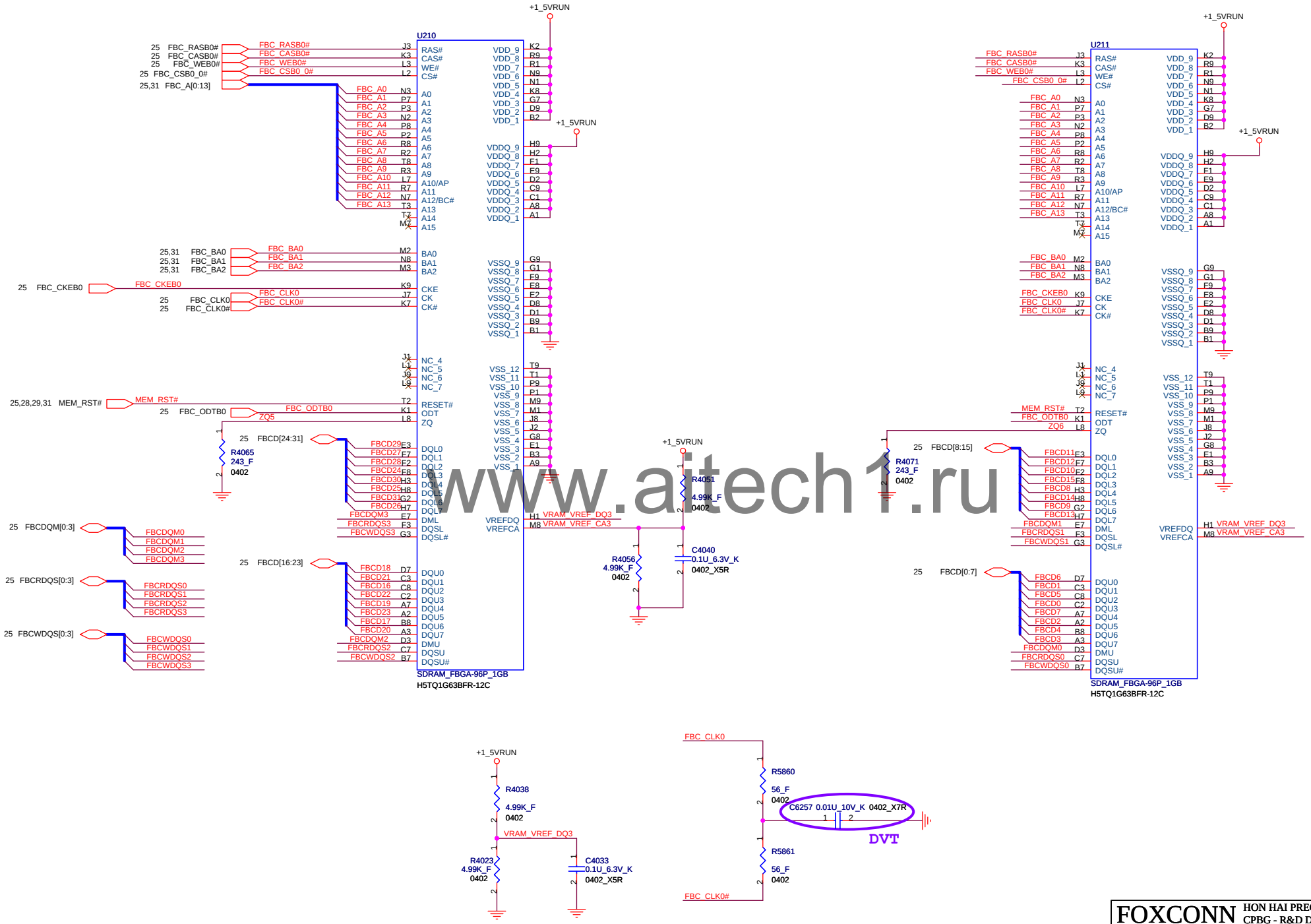
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM(DDR)# 2/4

Size: A3 | Document Number: M960&M970 H Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 29 of 86



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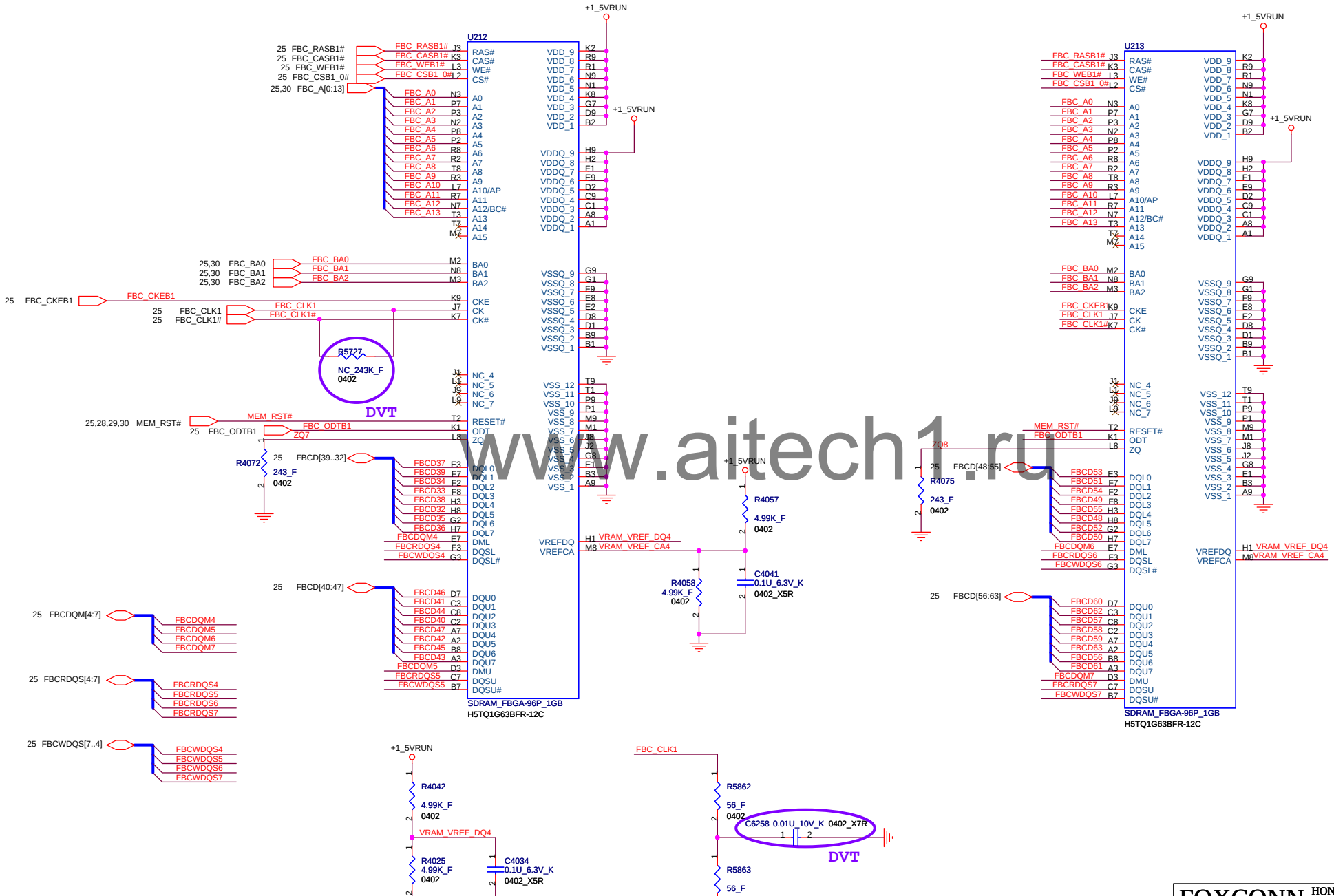
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM(DDR)# 3/4
Size A3	Document Number M960&M970 H Model
Rev	SA
Date: Tuesday, December 29, 2009	Sheet 30 of 86



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FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM(DDR)# 4/4
Size A3	Document Number M960&M970 H Model
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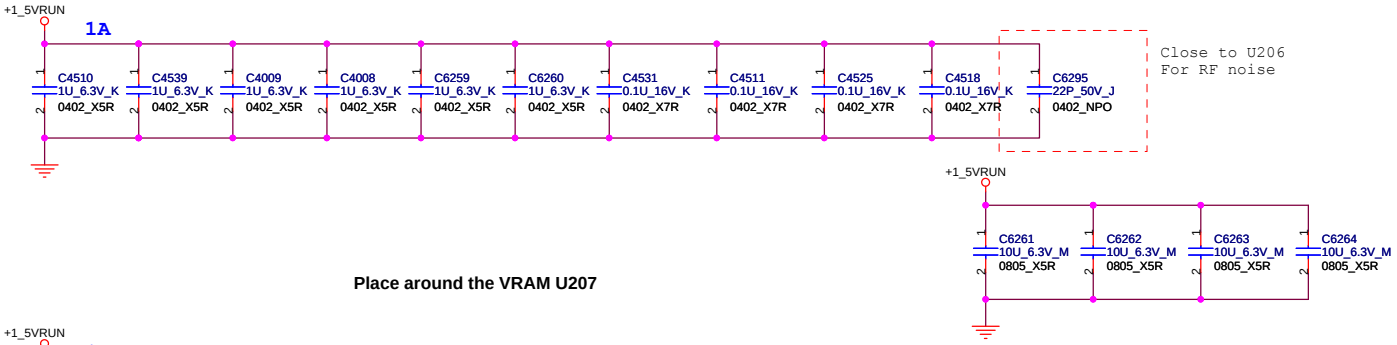
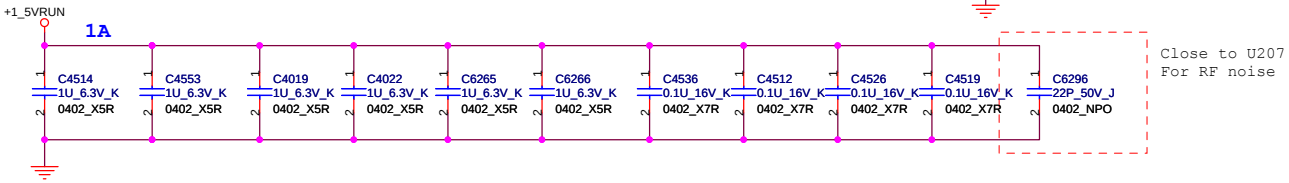
Date: Tuesday, December 29, 2009	Sheet 31 of 86

Place around the VRAM U206



Place around the VRAM U207



Place around the VRAM U208

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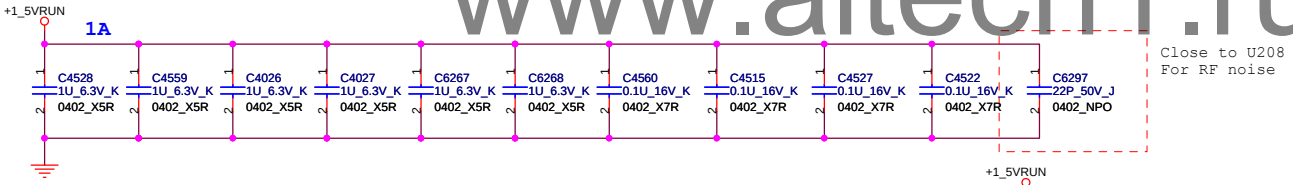
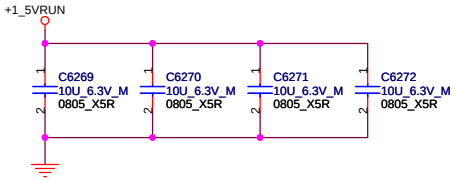
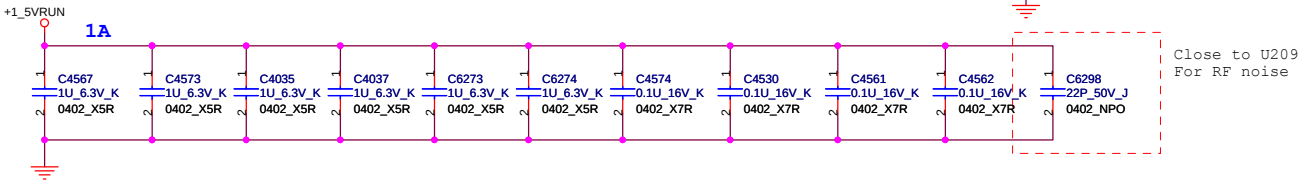


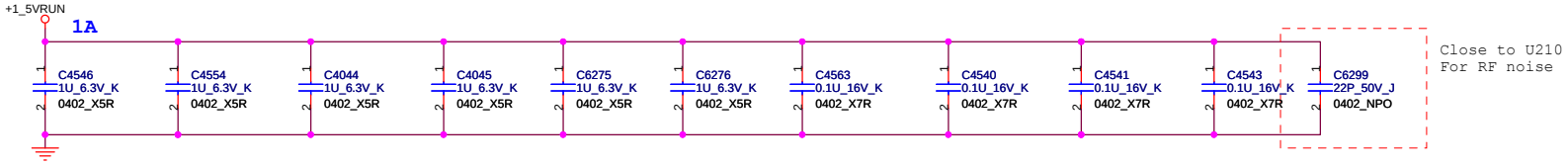


Place around the VRAM U209

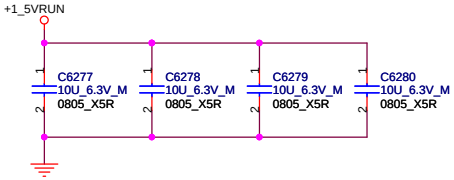


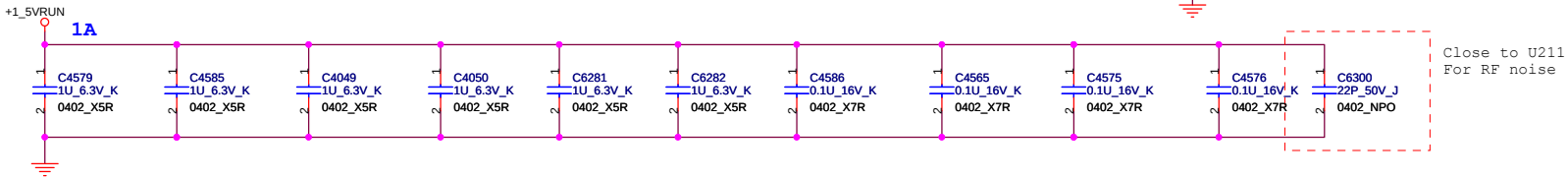
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(N11M BYPASS) 1/2	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 32 of 86	

Place around the VRAM U210



Place around the VRAM U211





Place around the VRAM U212

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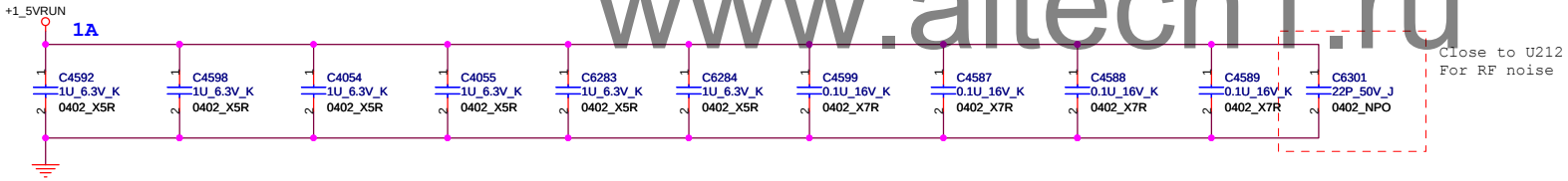
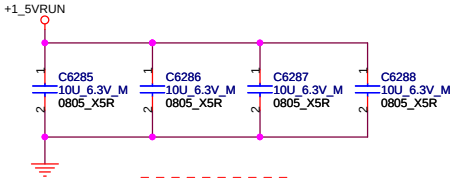
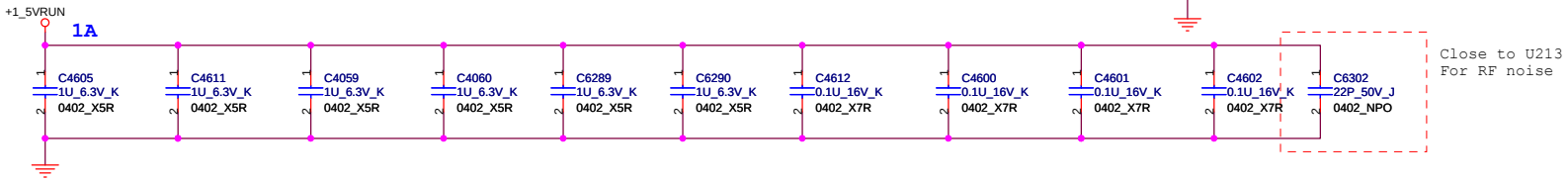
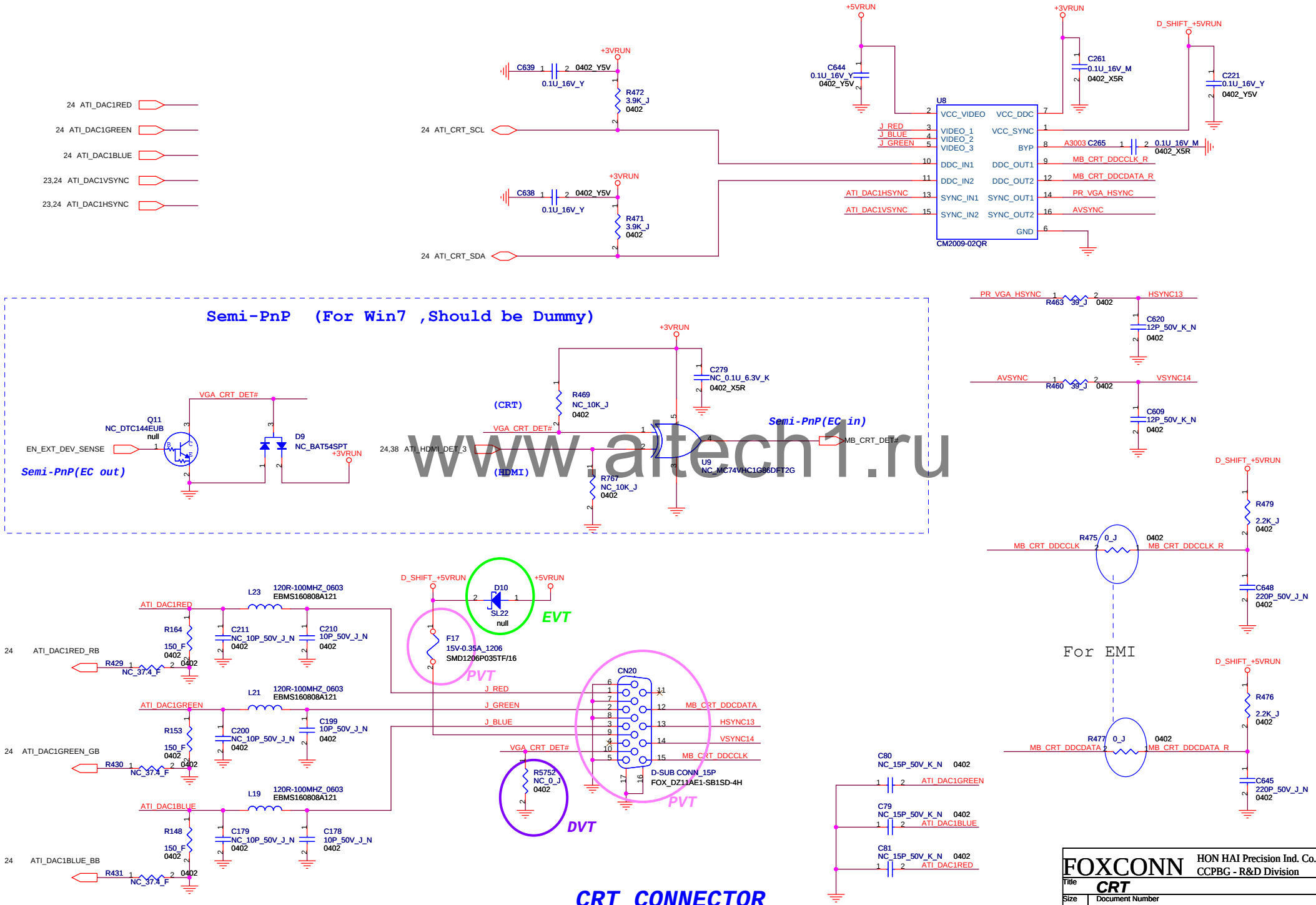


Place around the VRAM U213





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(N11P BYPASS) 2/2	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 33 of 86	



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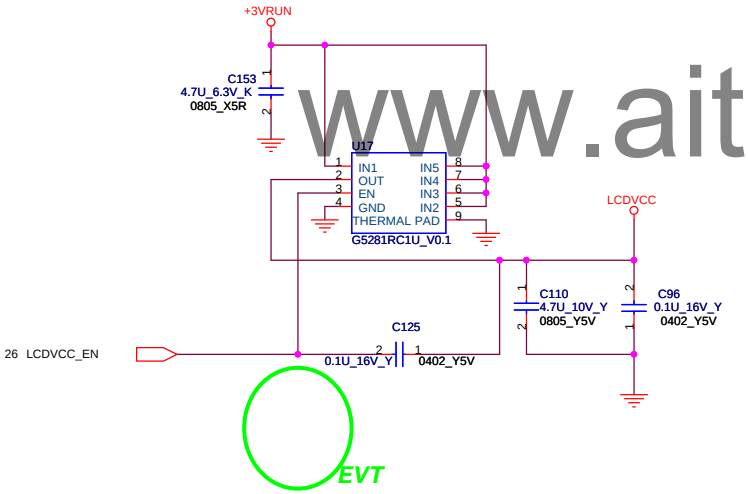
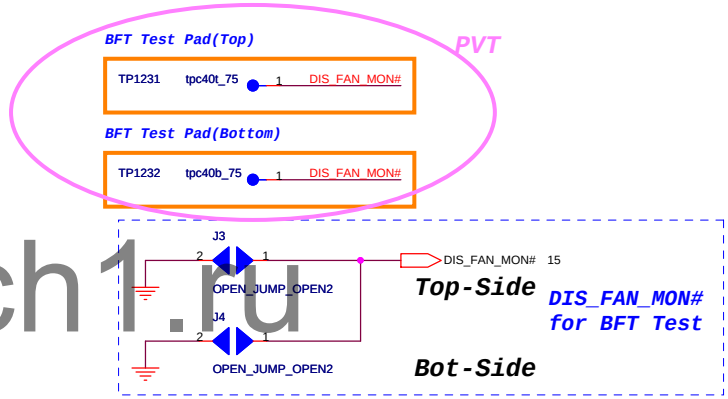
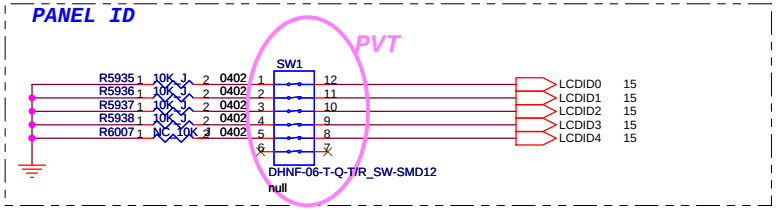
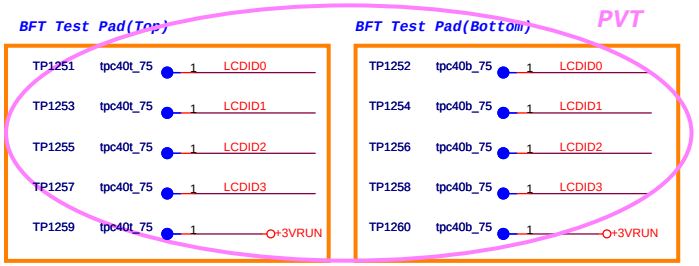
LVDS









PANEL ID

Type		LED	LED	LED	LED	1	1	1	LED	LED	LED
Size	14	14	14	14	14	15.5	15.5	15.5	15.5	17.3	17.3
Vendor	No LCD	AUO	Samsung	LGD	AUO	LGD	CPT	Samsung	LGD	CPT	AUO
Model Name		B140XW02	LTN140AT08	LP140WH2	B140RW02	LP156WH1	CLAA156WA01A	LTN156AT01	LP156WF1	CLAA173UA01A	B173HW01
Panel ID [4.3.2.1.0]	00000	00001	00010	00011	00100	00110	00111	01000	01001	01011	01100

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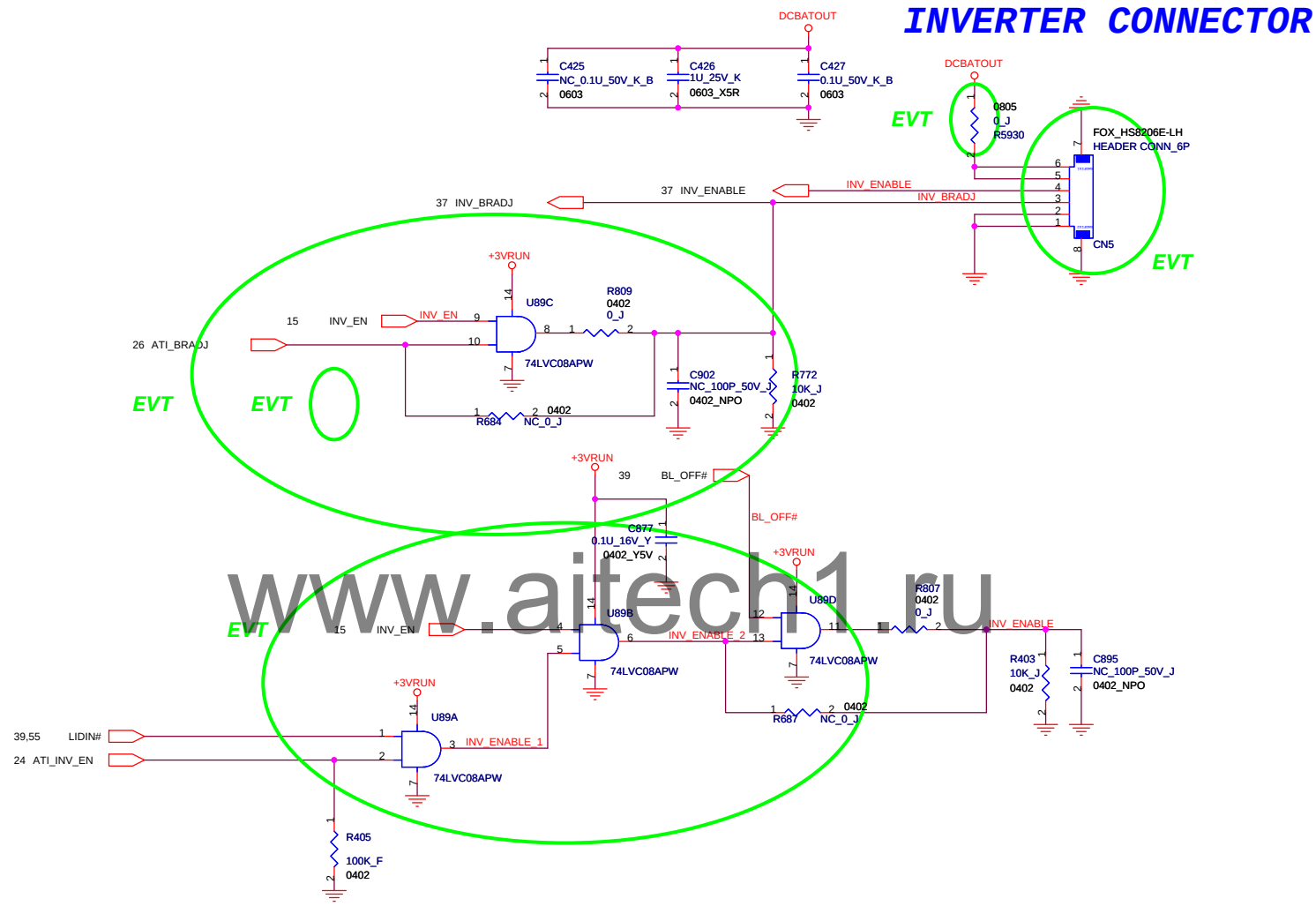
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: LVDS

Size: A3 | Document Number: M960&M970 H Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 35 of 86

INVERTER CONNECTOR



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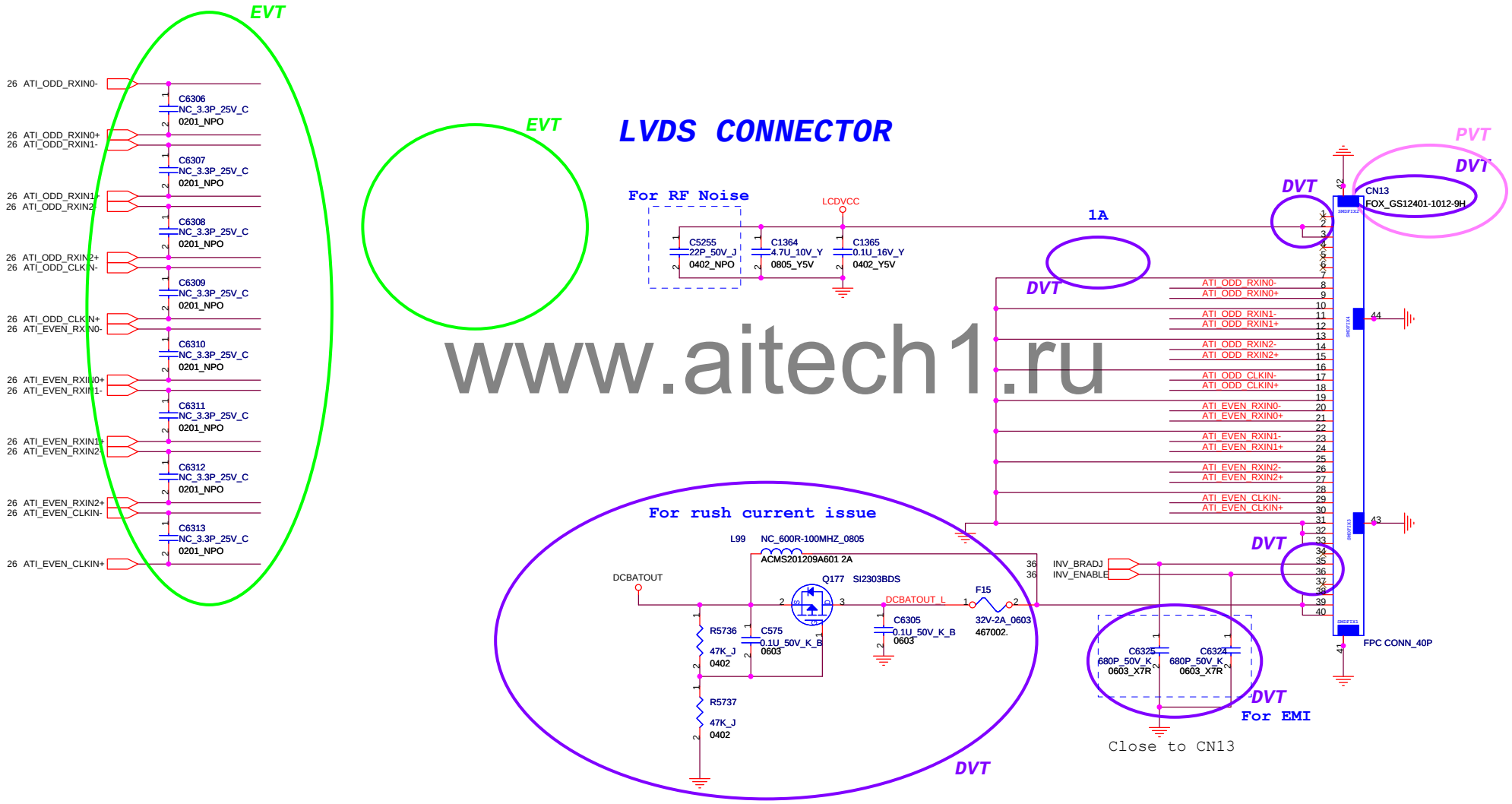
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	INVERTER CONNECTOR	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 36 of 86	

For RF verification, del these cap. in DVT if these cap. do not use.



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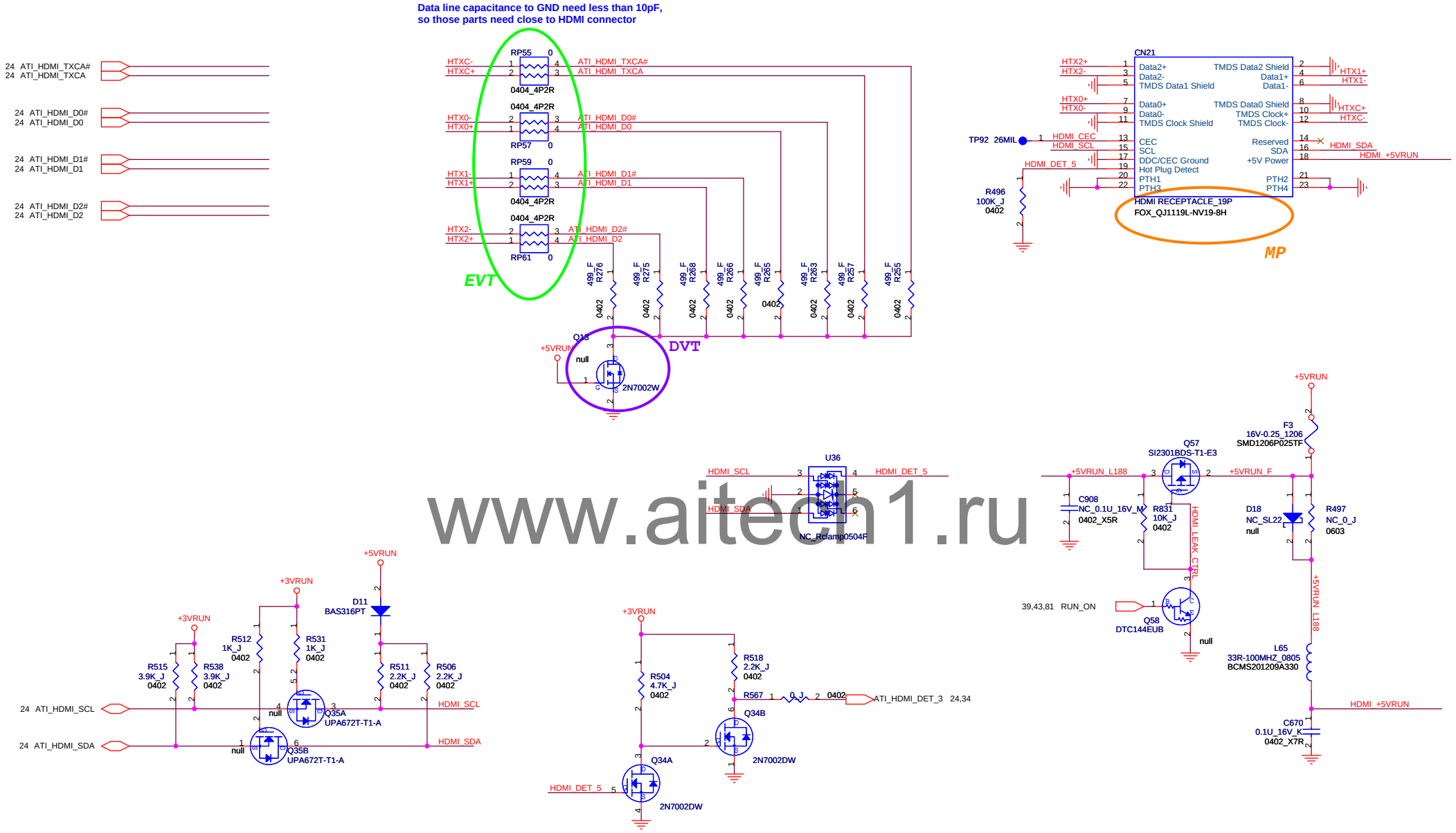
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LVDS Connector	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 37 of 86	



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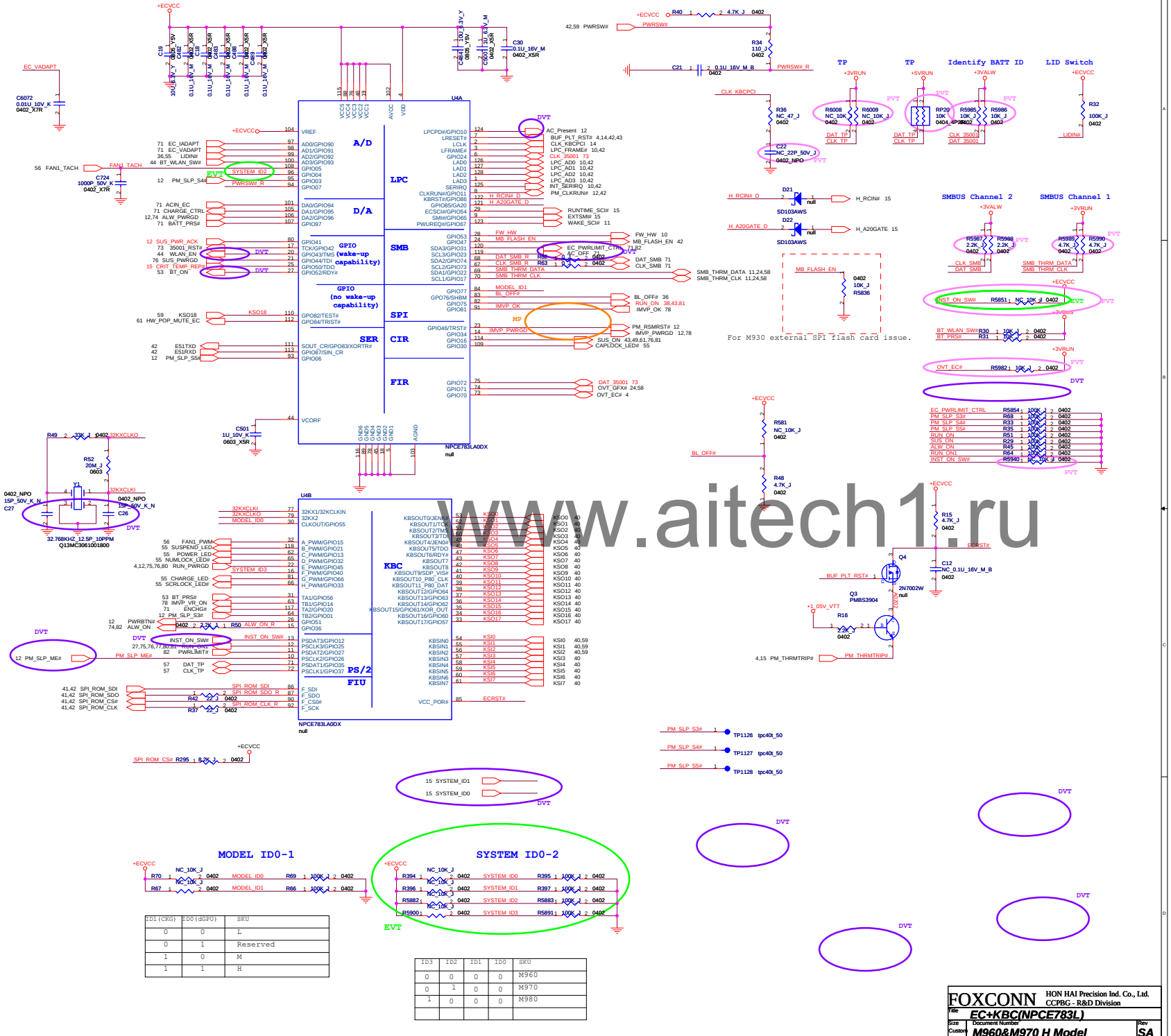
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 38 of 86	



ID1(CKG)	ID0(dGPU)	SKU
0	0	L
0	1	Reserved
1	0	M
1	1	H

ID3	ID2	ID1	ID0	SKU
0	0	0	0	M960
0	1	0	0	M970
1	0	0	0	M980

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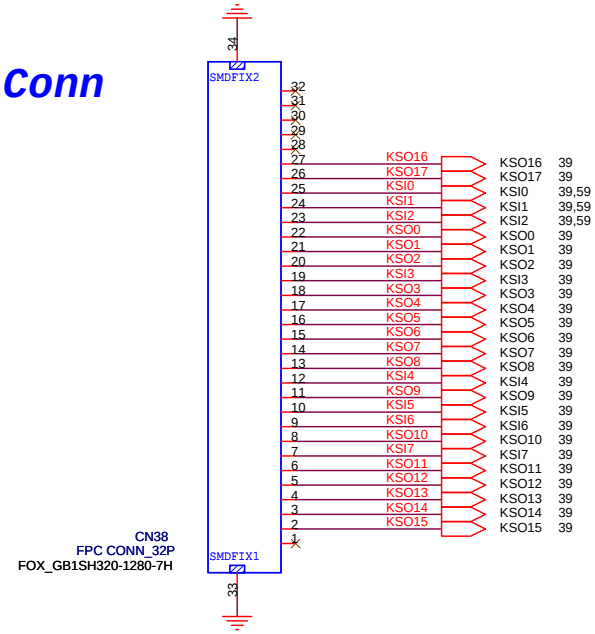
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	EC+KBC(NPCE783L)
Size / Document Number	M960&M970 H Model
Rev	SA
Custom	
Date: Tuesday, December 29, 2009	Sheet 39 of 86

KBC Conn



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BFT Test Pad(Top)

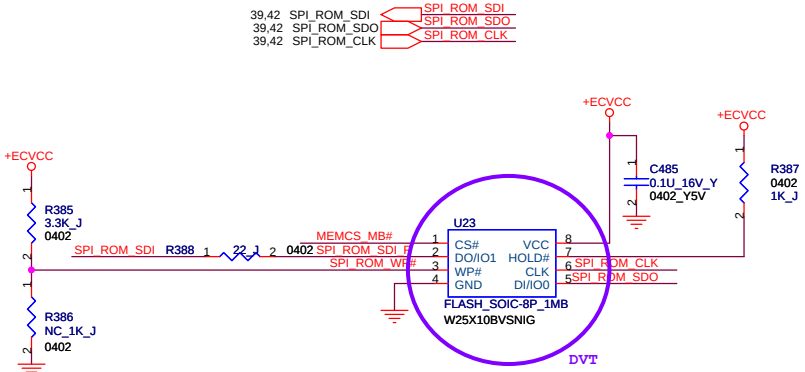
TP1198	tpc40t_75	1	KSI7
TP1200	tpc40t_75	1	KSO10
TP1202	tpc40t_75	1	KSO6
TP1204	tpc40t_75	1	KSI2
TP1206	tpc40t_75	1	KSI0
TP1233	tpc40t_75	1	KSI3
TP1234	tpc40t_75	1	KSO13

PVT

BFT Test Pad(Bottom)

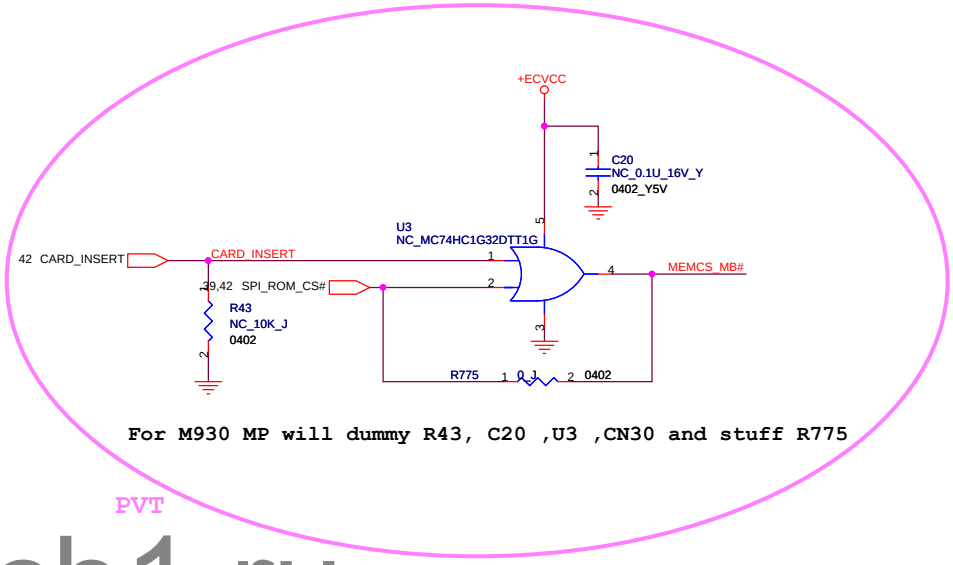
TP1199	tpc40b_75	1	KSI7
TP1201	tpc40b_75	1	KSO10
TP1203	tpc40b_75	1	KSO6
TP1205	tpc40b_75	1	KSI2
TP1207	tpc40b_75	1	KSI0

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	KB Connector	
Size B	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 40 of 86	



SPI ROM (EC Firmware)

SPI ROM (EC Firmware) (1Mb)



For M930 MP will dummy R43, C20 ,U3 ,CN30 and stuff R775

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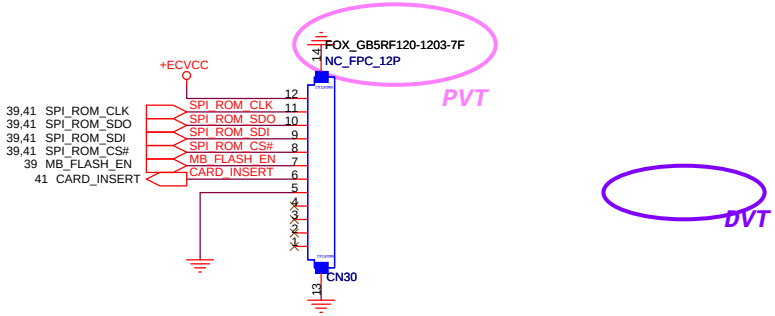
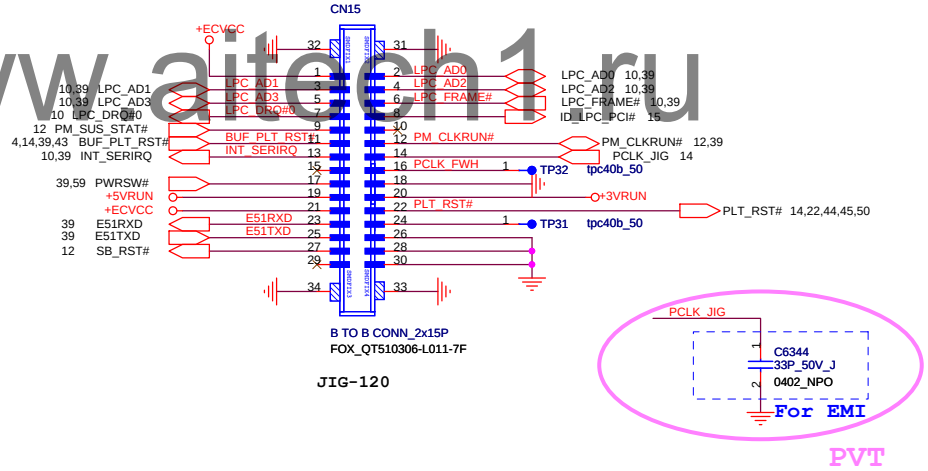
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SPI Flash ROM	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 41 of 86	



EXTERNAL SPI ROM INTERFACE (EC)



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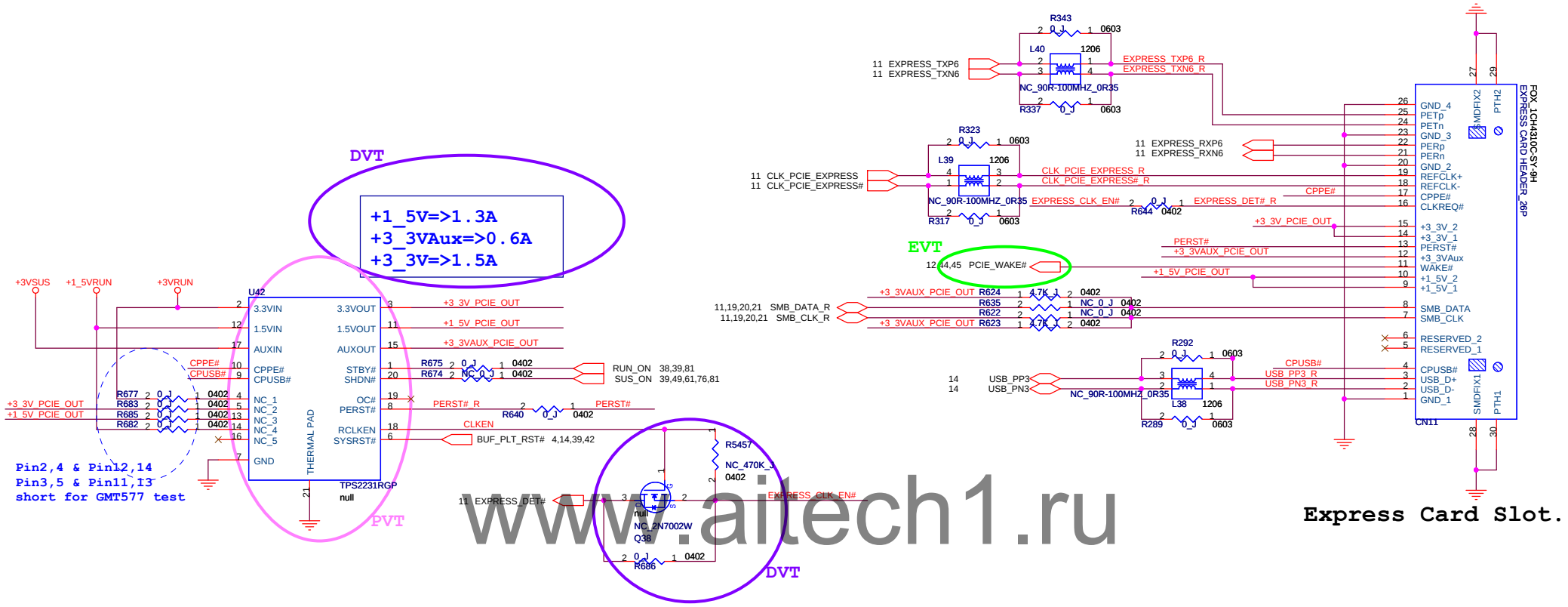
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Debug Port	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 42 of 86	



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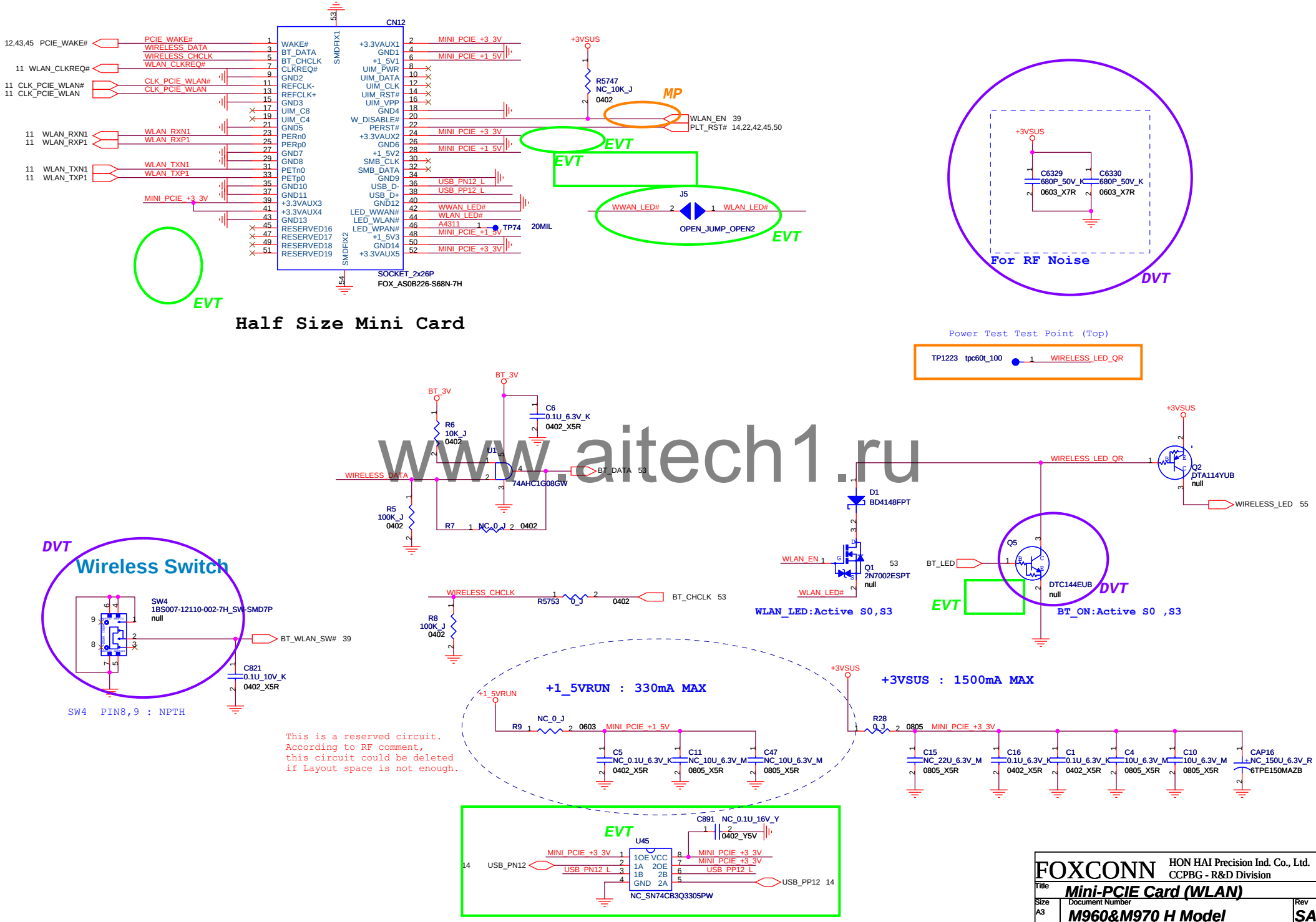
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EXPRESS CARD	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 43 of 86	



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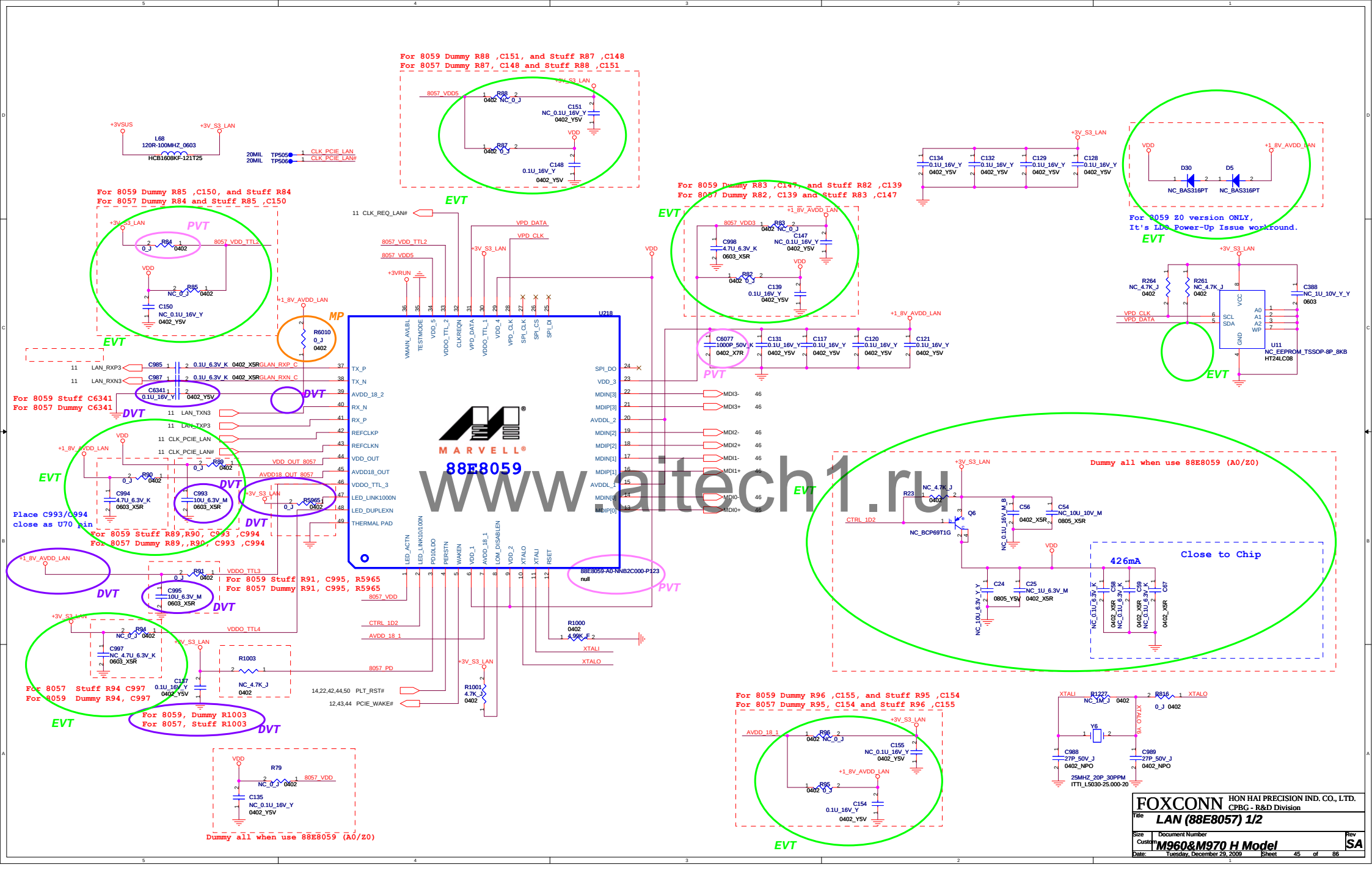
For 8059 Dummy R88 ,C151, and Stuff R87 ,C148
For 8057 Dummy R87, C148 and Stuff R88 ,C151
For 8059 Dummy R85 ,C150, and Stuff R84
For 8057 Dummy R84 and Stuff R85 ,C150
For 8059 Dummy R83 ,C147, and Stuff R82 ,C139
For 8057 Dummy R82, C139 and Stuff R83 ,C147
For 8059 Z0 version ONLY,
It's LDO Power-Up Issue workround.
For 8059 Stuff C6341
For 8057 Dummy C6341
Place C993/C994
close as U70 pin
For 8059 Stuff R89,R90, C993 ,C994
For 8057 Dummy R89,,R90, C993 ,C994
For 8059 Stuff R91, C995, R5965
For 8057 Dummy R91, C995, R5965
For 8057 Stuff R94 C997
For 8059 Dummy R94, C997
For 8059, Dummy R1003
For 8057, Stuff R1003
For 8059 Dummy R96 ,C155, and Stuff R95 ,C154
For 8057 Dummy R95, C154 and Stuff R96 ,C155
Dummy all when use 88E8059 (A0/Z0)
Dummy all when use 88E8059 (A0/Z0)
426mA
Close to Chip
MARVELL
88E8059
EVT
DVT
PVT
MP
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FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
LAN (88E8057) 1/2
M960&M970 H Model
SA
Tuesday, December 29, 2009
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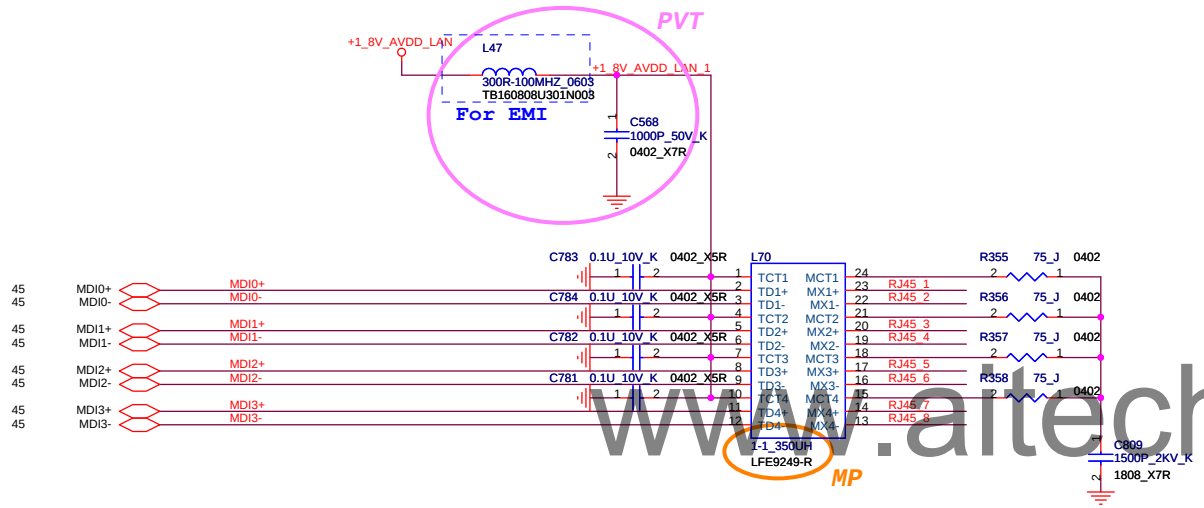

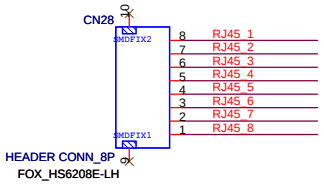

RJ45

BFT Test Point(TOP)

TP1166	tpc40t_75	1	RJ45_8	TP1174	tpc40t_75	1	RJ45_4
TP1168	tpc40t_75	1	RJ45_7	TP1176	tpc40t_75	1	RJ45_3
TP1170	tpc40t_75	1	RJ45_6	TP1178	tpc40t_75	1	RJ45_2
TP1172	tpc40t_75	1	RJ45_5	TP1180	tpc40t_75	1	RJ45_1

BFT Test Point(Bottom)

TP1167	tpc40b_75	1	RJ45_8	TP1175	tpc40b_75	1	RJ45_4
TP1169	tpc40b_75	1	RJ45_7	TP1177	tpc40b_75	1	RJ45_3
TP1171	tpc40b_75	1	RJ45_6	TP1179	tpc40b_75	1	RJ45_2
TP1173	tpc40b_75	1	RJ45_5	TP1181	tpc40b_75	1	RJ45_1

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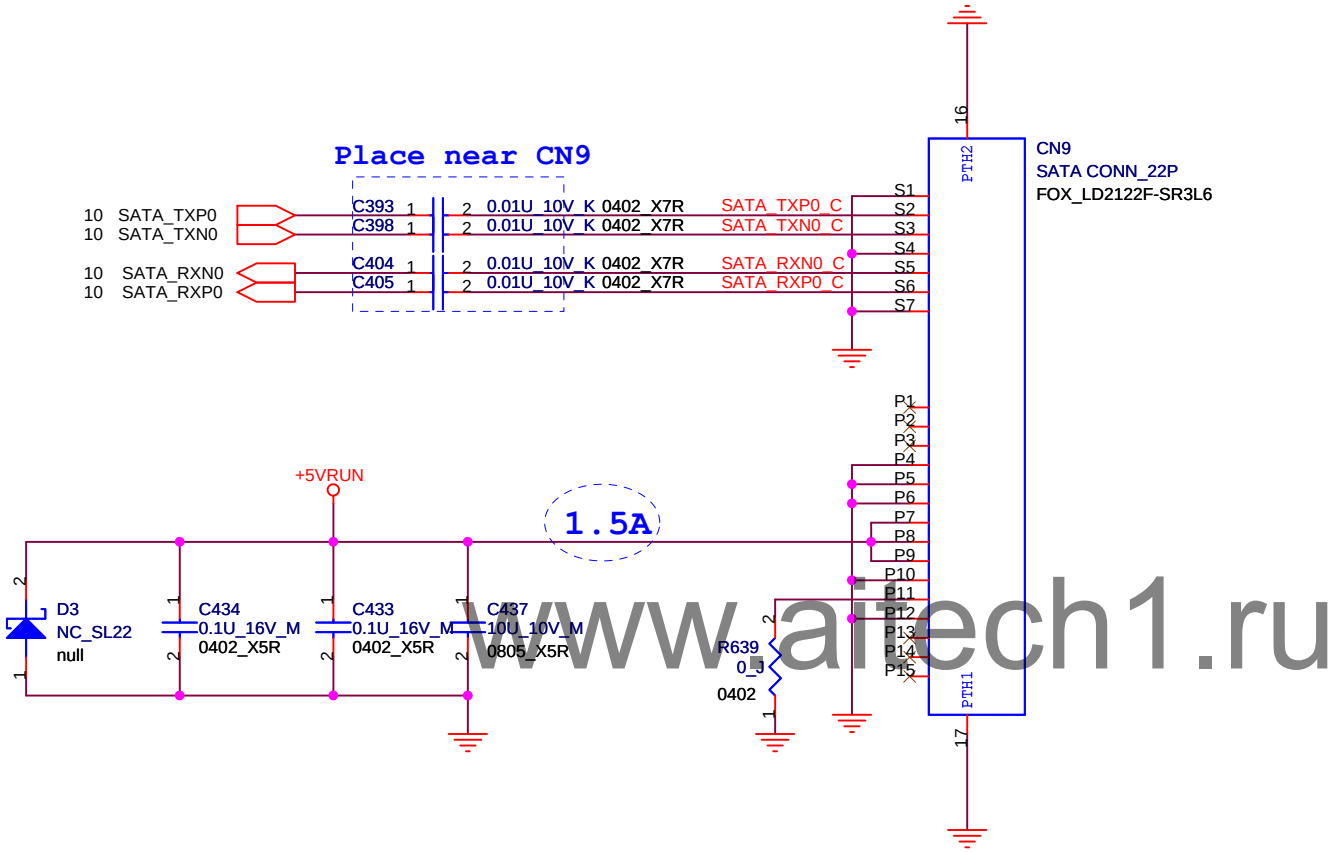
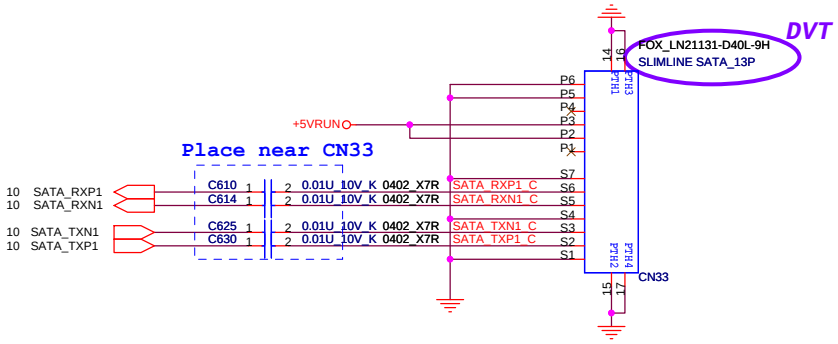
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN (Transfomer)(2/2)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 46 of 86	



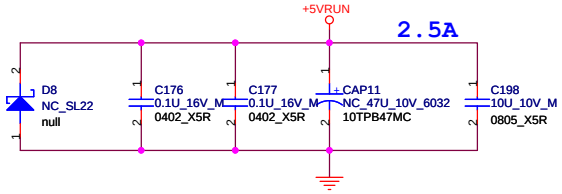
www.airech1.ru

SATA HDD CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA HDD	
Size A4	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 47 of 86	



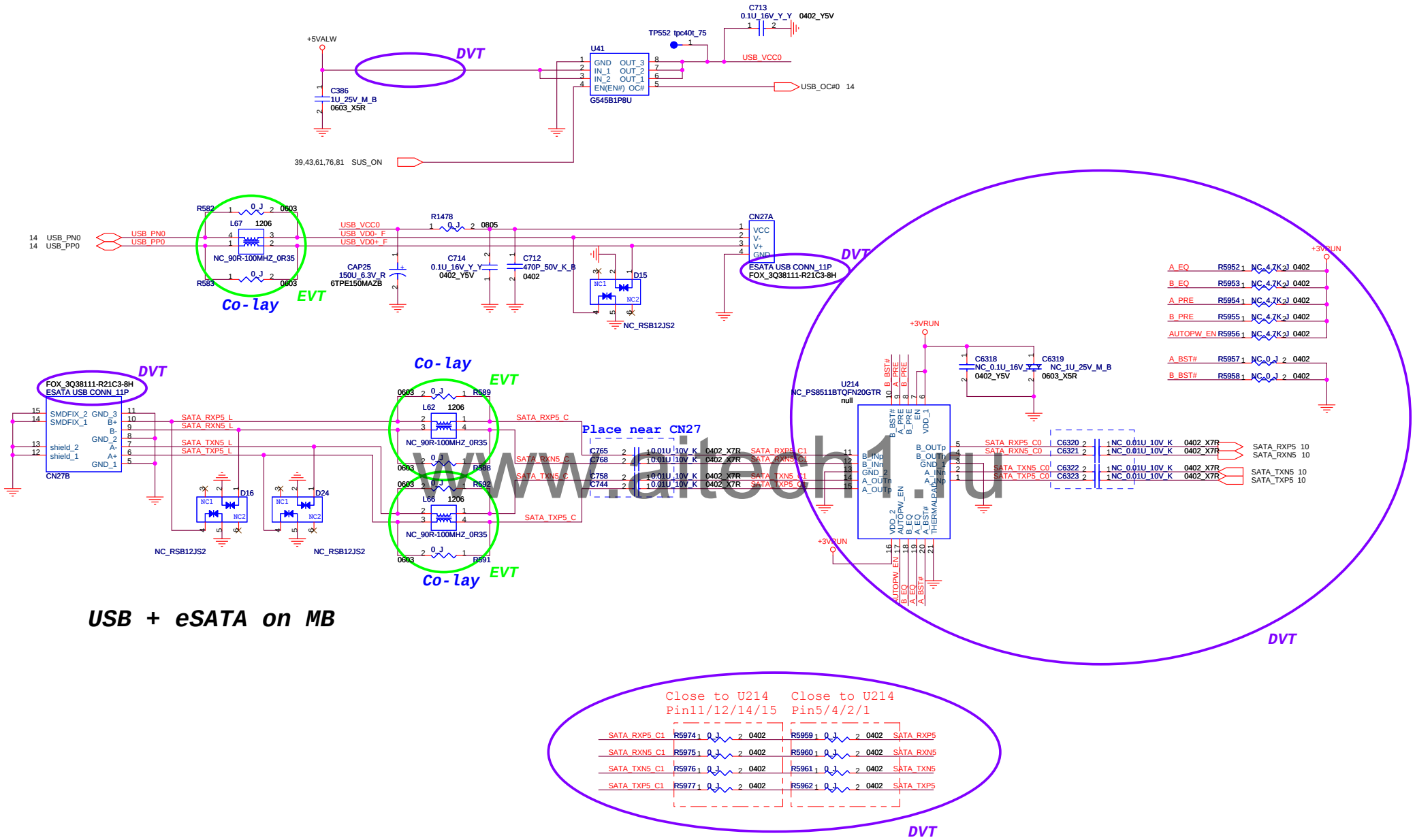
SATA ODD CONN



www.aitech1.ru

DVT

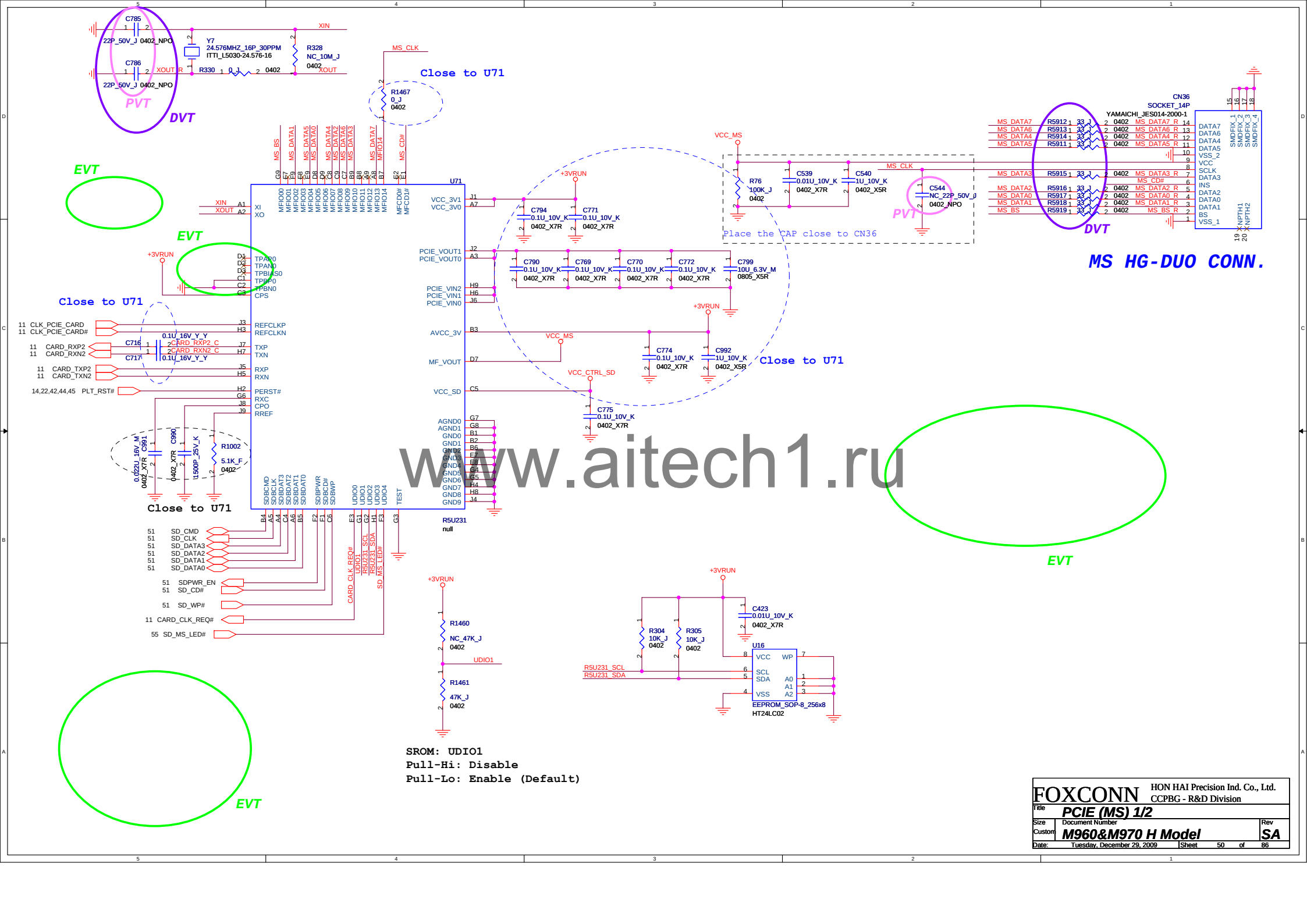
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA ODD	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 48 of 86	



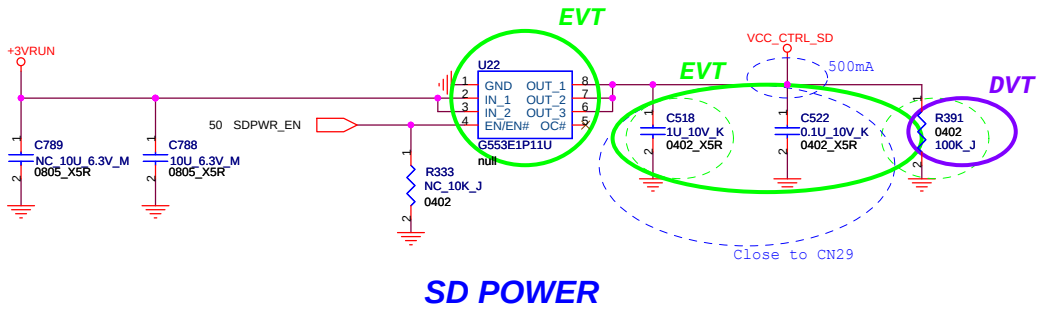
www.laptech1.ru

USB + eSATA on MB

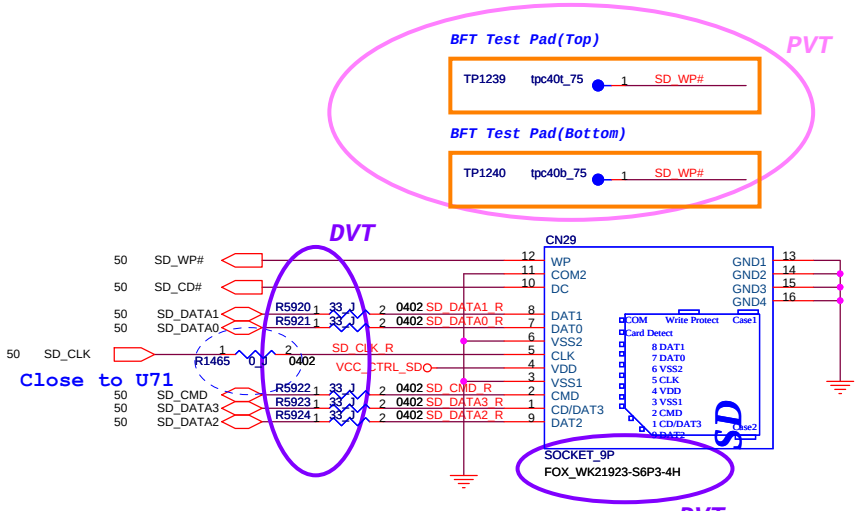
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	eSATA Combo	
Size: Custom	Document Number: M960&M970 H Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 49 of 86	



www.aitech1.ru



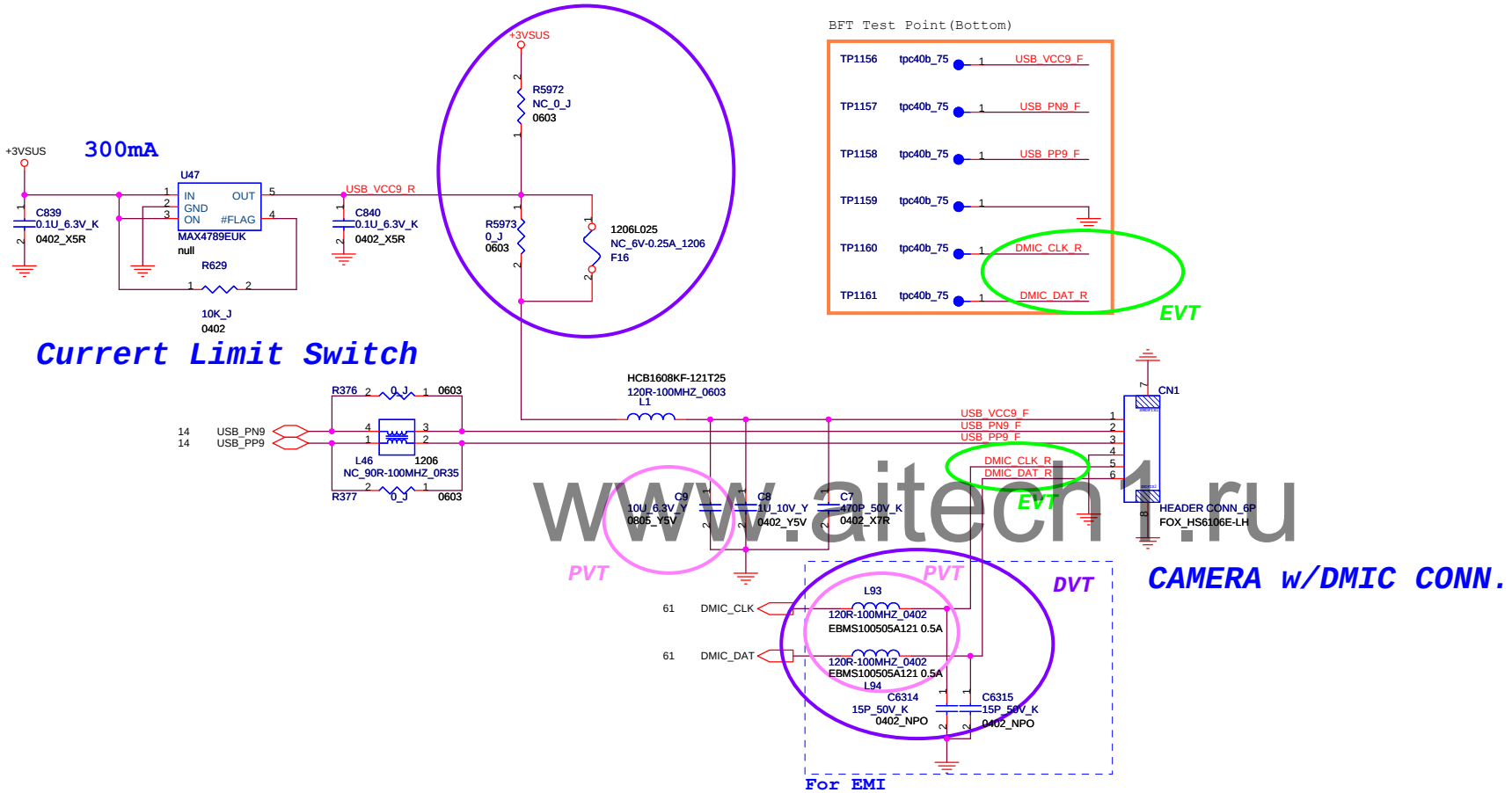
SD POWER



SD CONN.

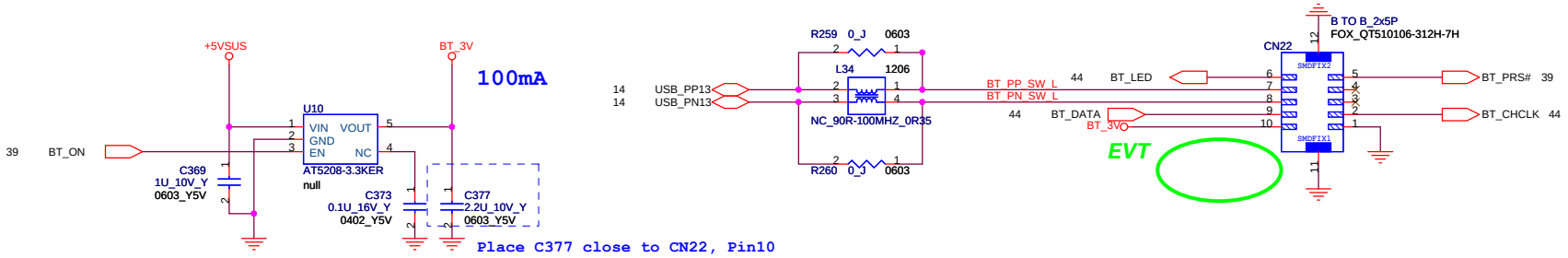
www.aitech1.ru

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCIE (SD) 2/2	
Size Custom	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 51 of 86	



www.aitech1.ru

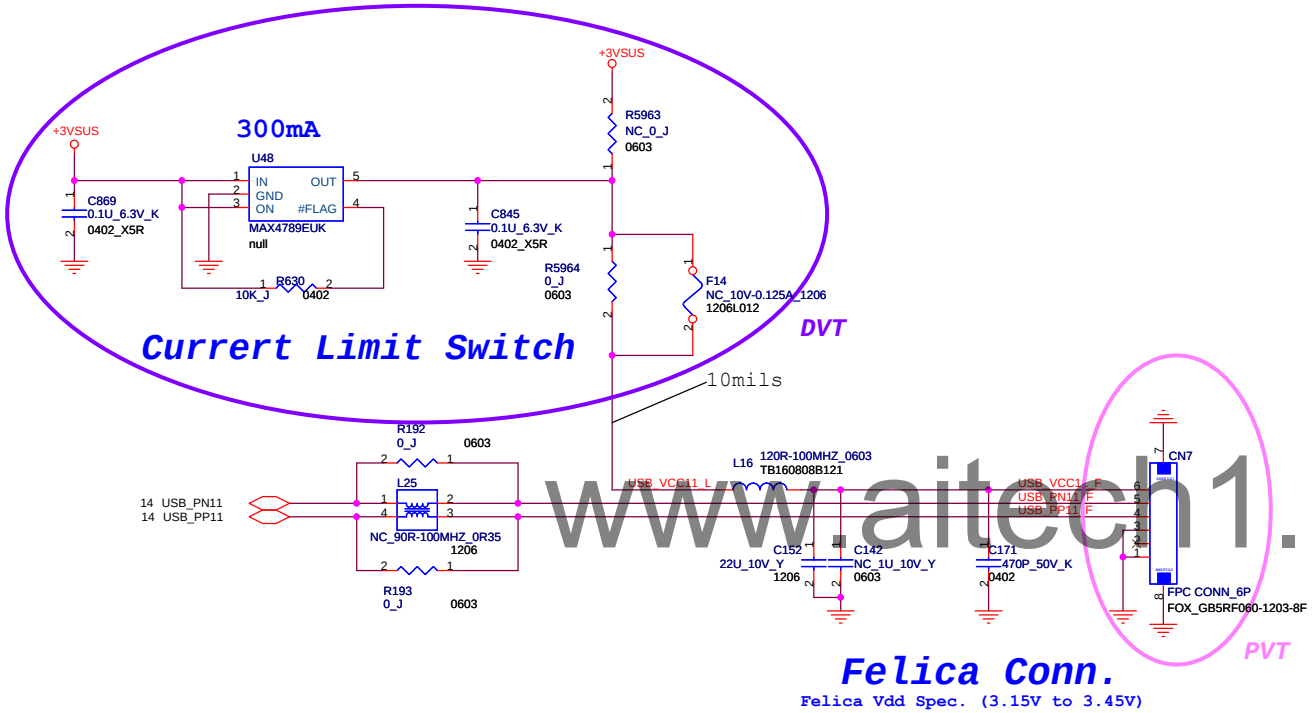
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Camera w/DMIC Connector	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 52 of 86	



Bluetooth CONN.

www.aitech1.ru

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Bluetooth Connector	
Size: Custom	Document Number: M960&M970 H Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 53 of 86	



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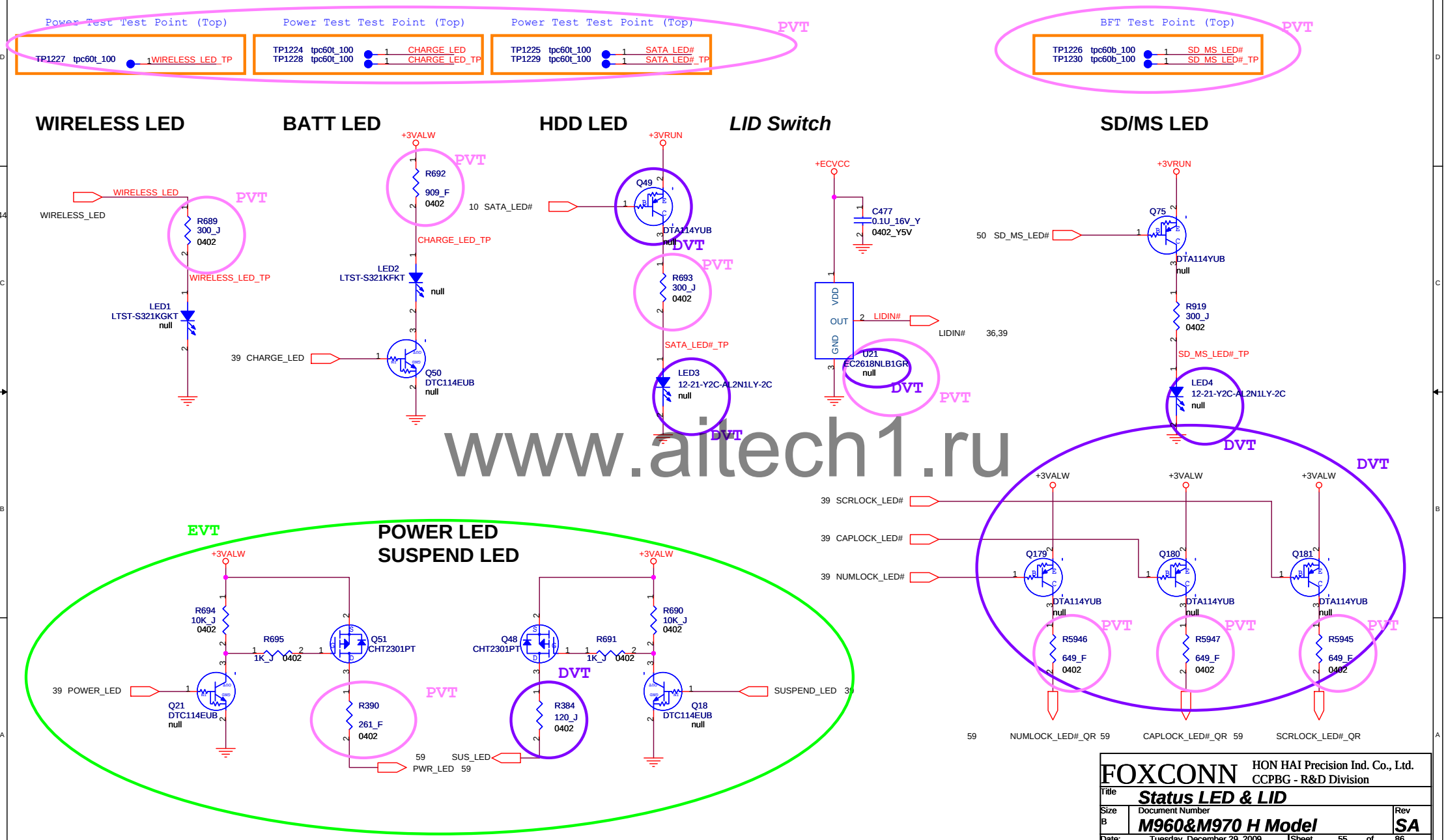
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Felica Connector	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 54 of 86	



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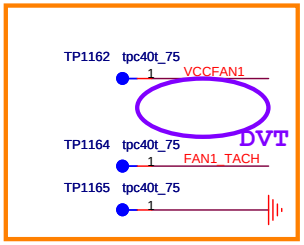
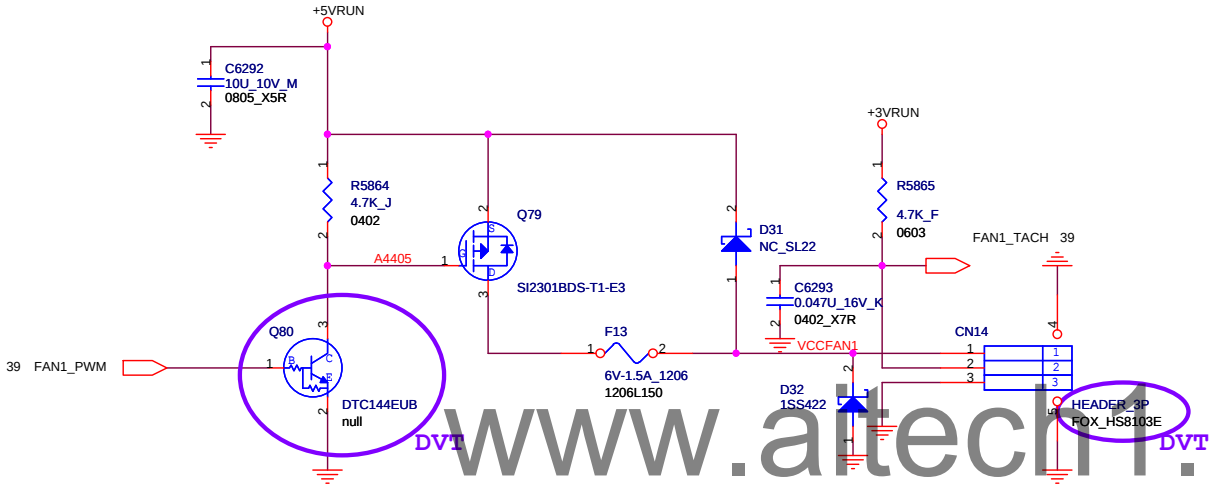
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Status LED & LID**	
Size B	Document Number **M960&M970 H Model**	Rev **SA**
Date: Tuesday, December 29, 2009	Sheet 55 of 86	



BFT Test Point(TOP)



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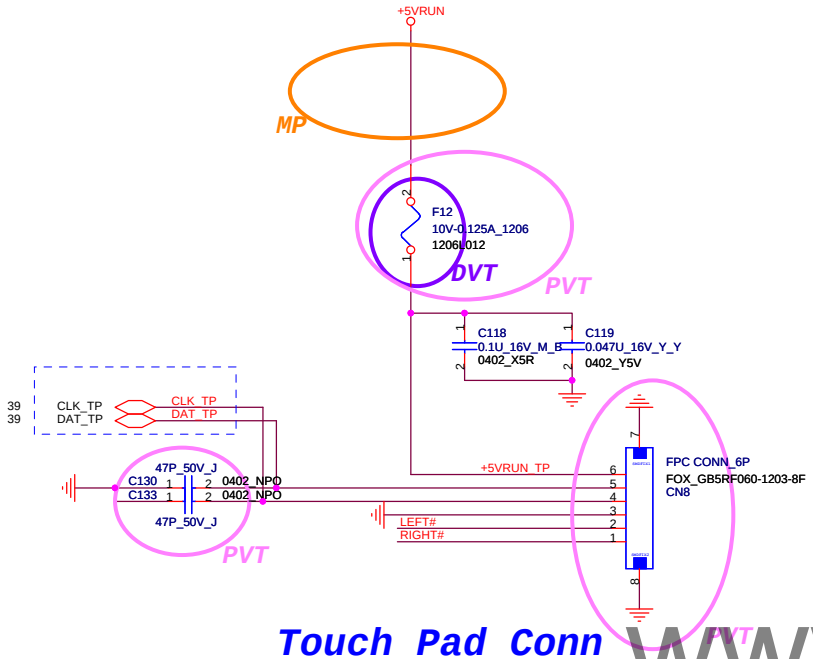
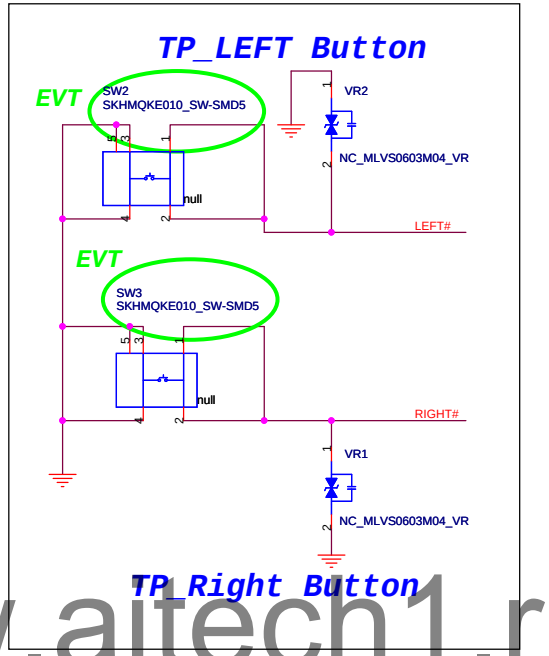
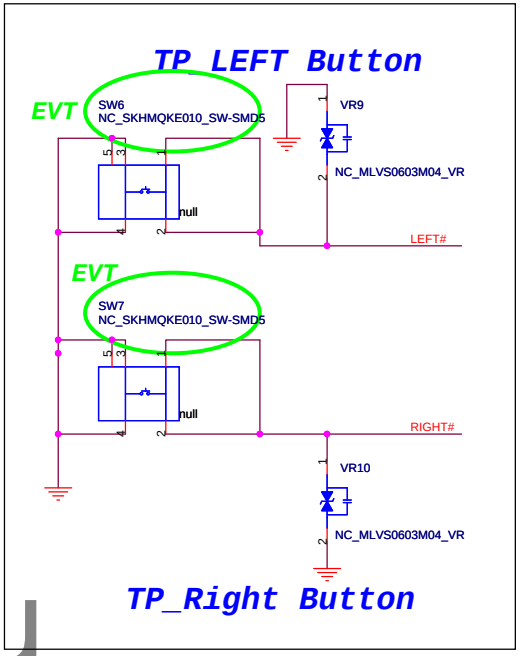
FAN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN	
Size B	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 56 of 86	





For M960 Only



For M970 Only

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M960/M970 T/P Control Table

	SW2	SW3	SW6	SW7				
M960	Stuff	Stuff	Dummy	Dummy				
M970	Dummy	Dummy	Stuff	Stuff				

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Touch Pad	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 57 of 86	

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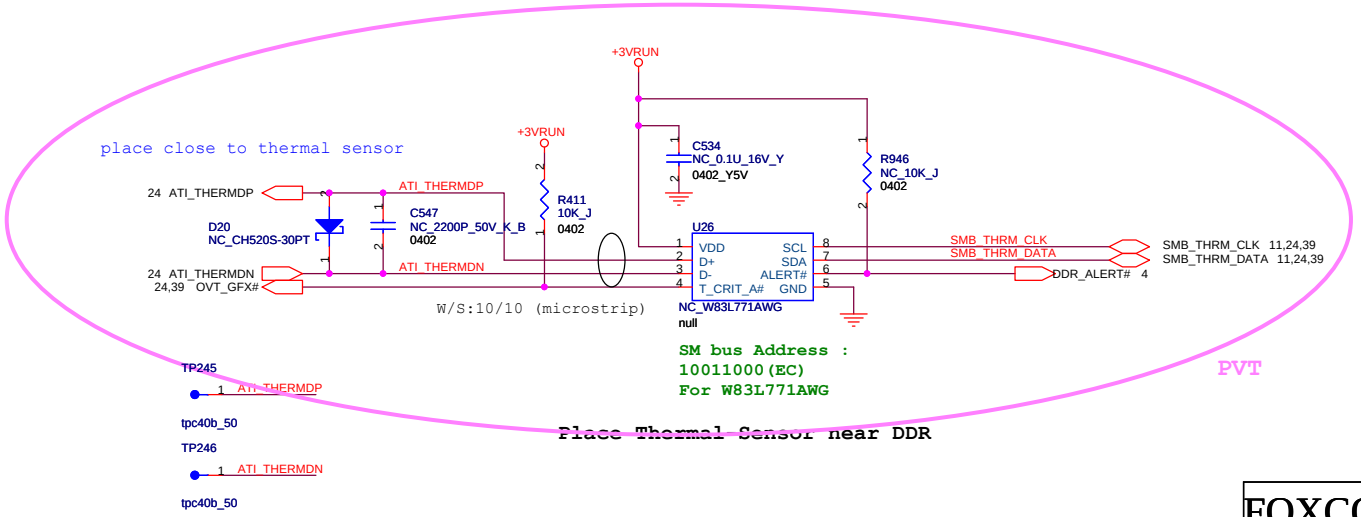
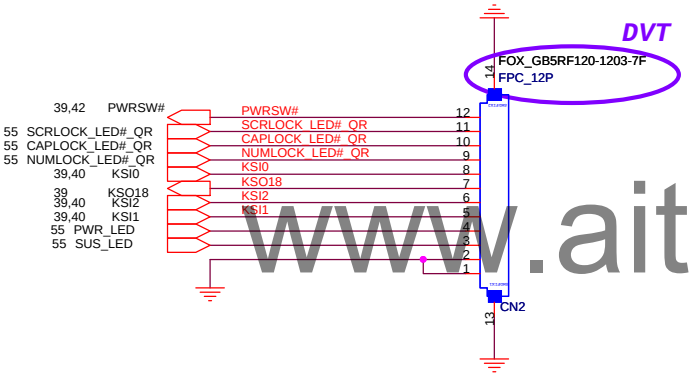
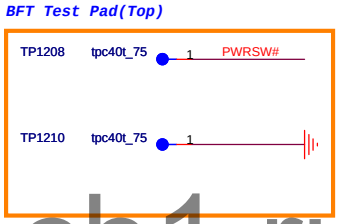
VGA Thermal SENSOR
W83L771AWG

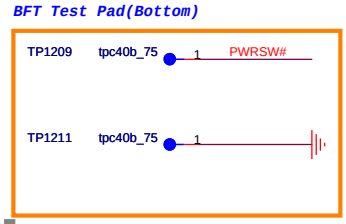


Place Thermal Sensor near DDR

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Thermal Sensor & Protection	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 58 of 86	







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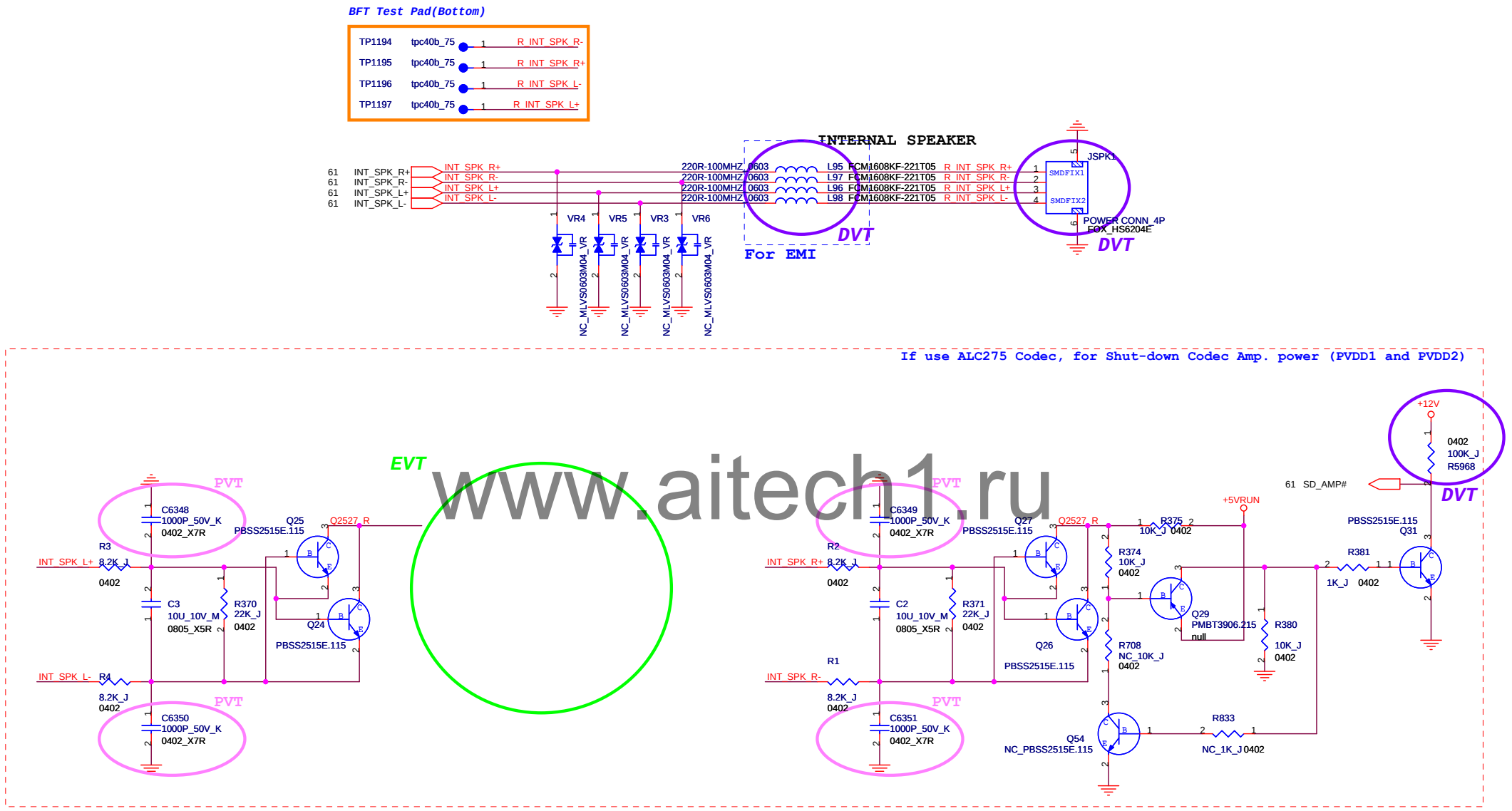
Switch DB Conn.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SWITCH DB Connector	
Size Custom	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 59 of 86	



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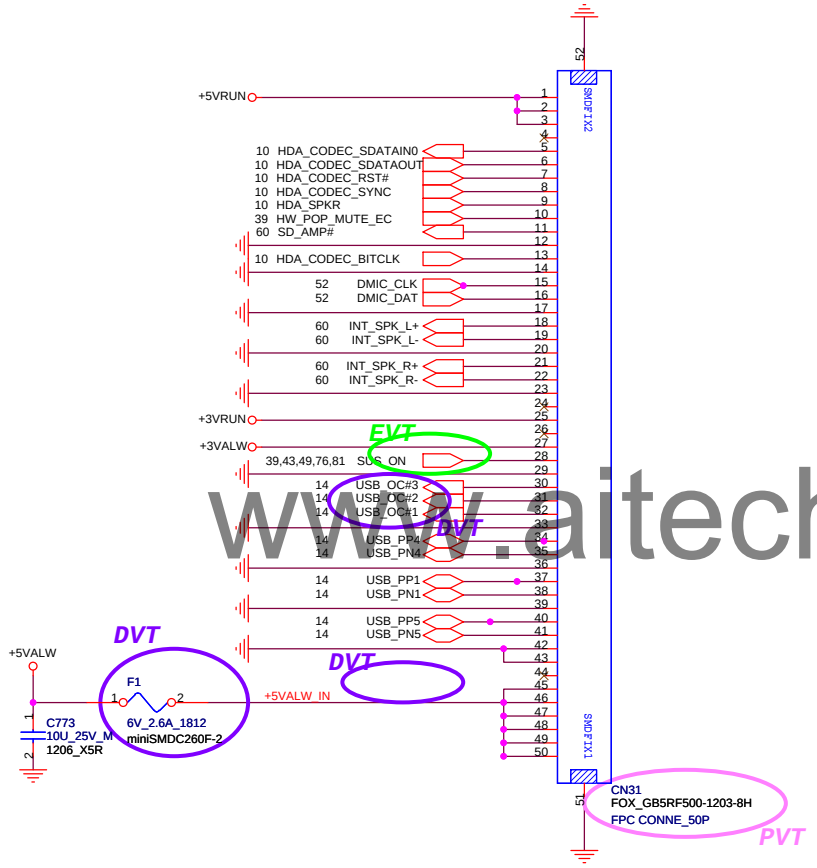
For Mor request,add the speaker cable short protection circuit

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO SPEAKER CONNECTOR	
Size B	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 60 of 86	



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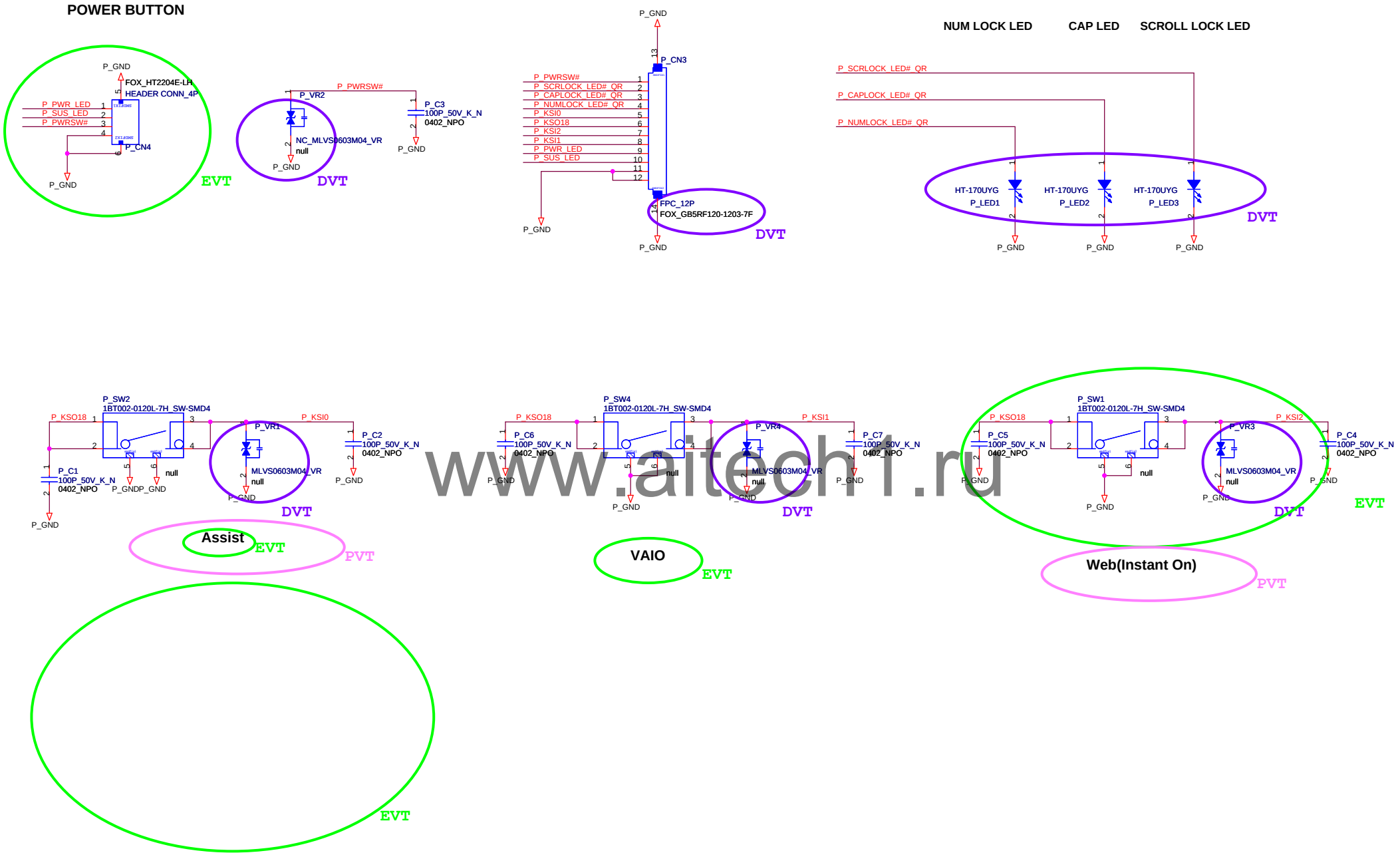
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO/USB DB Conn.	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 61 of 86	

Power Button Board



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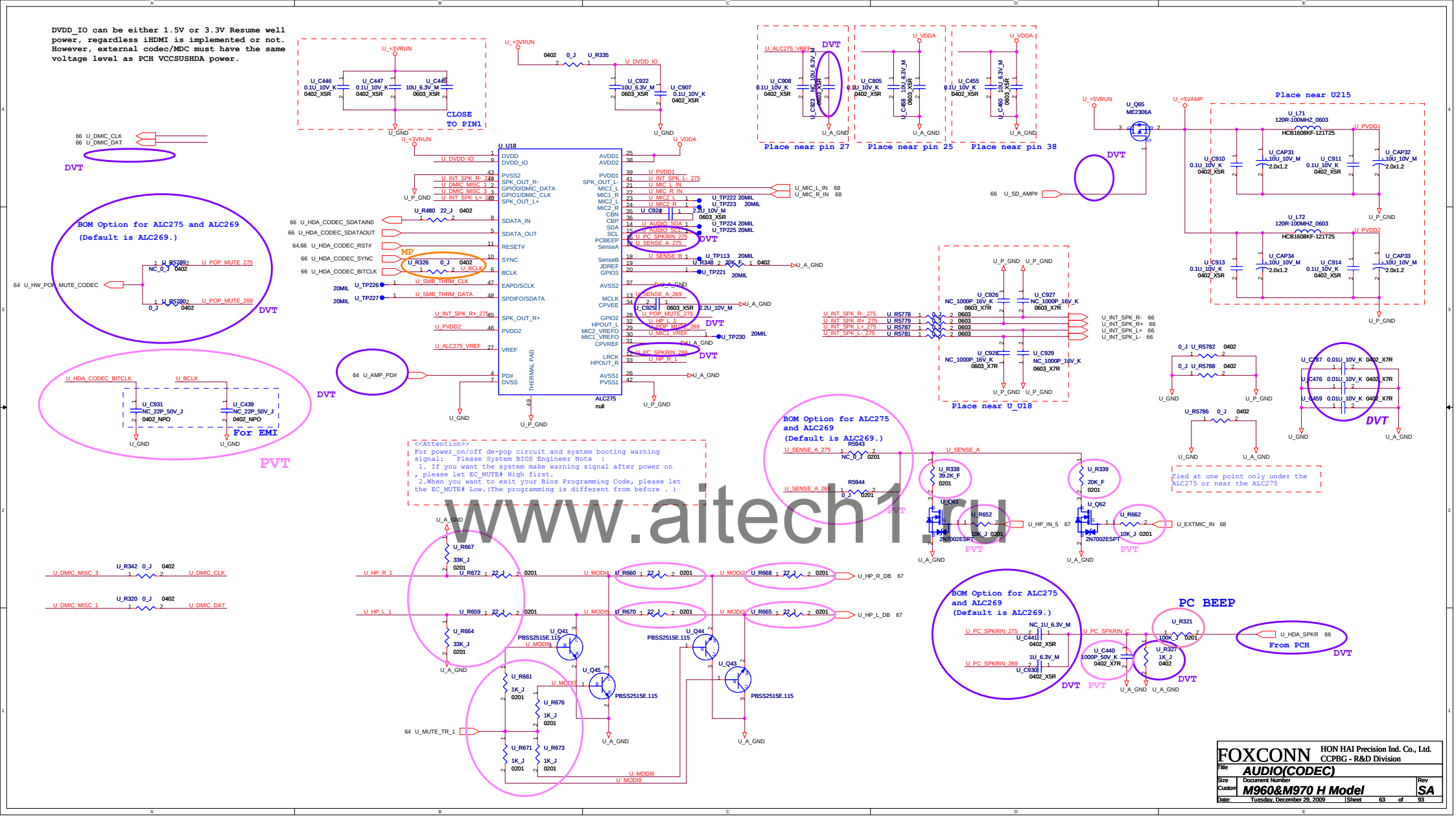
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SWITCH (BOTTON & KB LED)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 62 of 86	

DVDD_IO can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.



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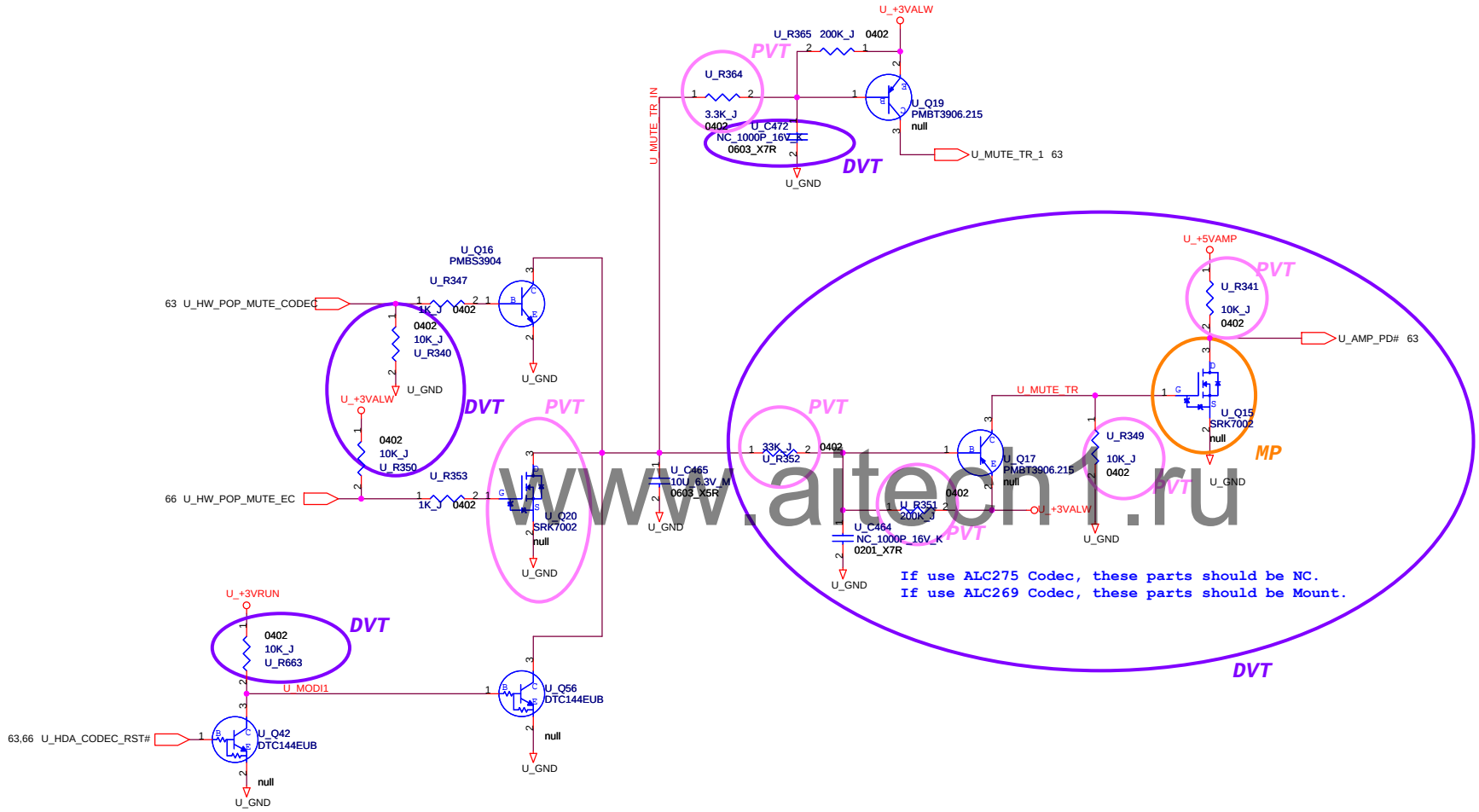
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO(CODEC)	
Size / Custom	Document Number: M960&M970 H Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 63 of 93	



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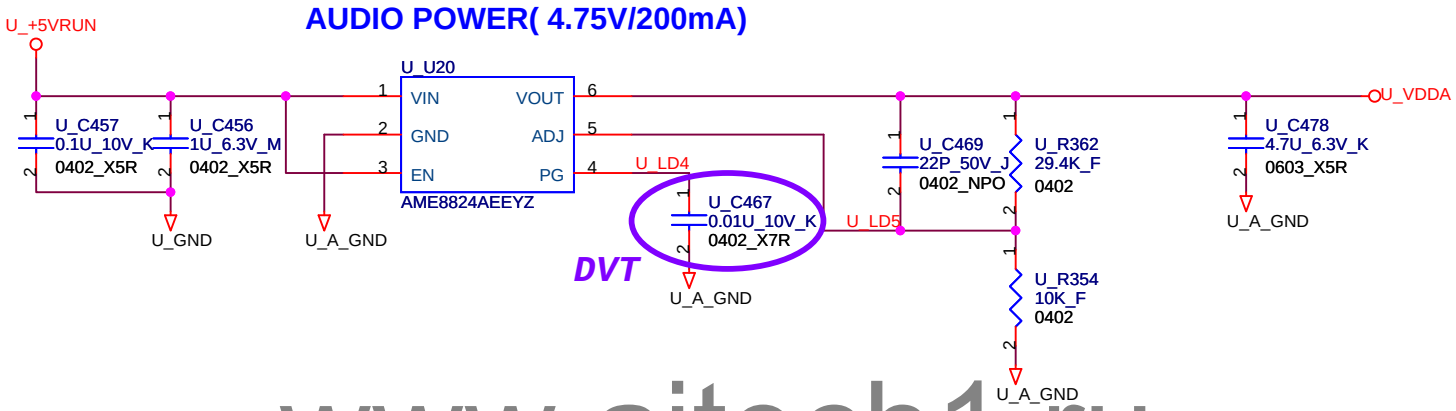
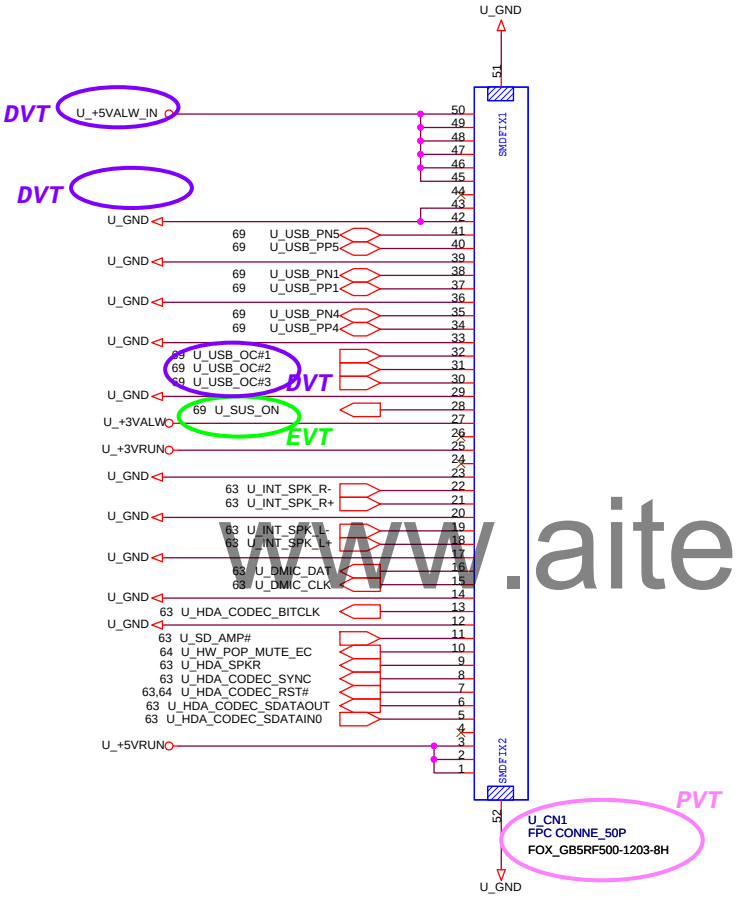
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO (MUTE)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 64 of 93	

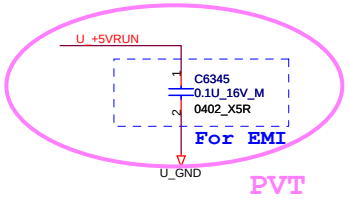
AUDIO POWER(4.75V/200mA)



www.aitech1.ru

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO POWER	
Size A4	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 65 of 93	





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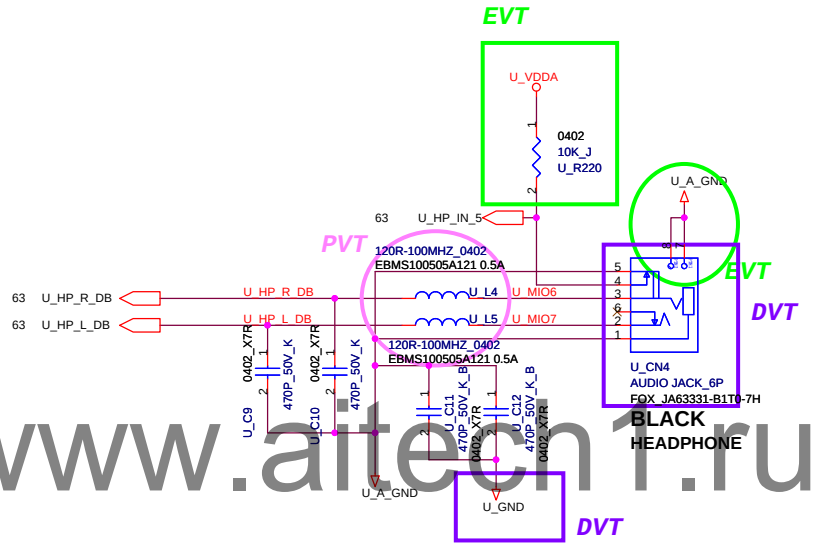
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (AUDIO & USB Conn)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 66 of 93	



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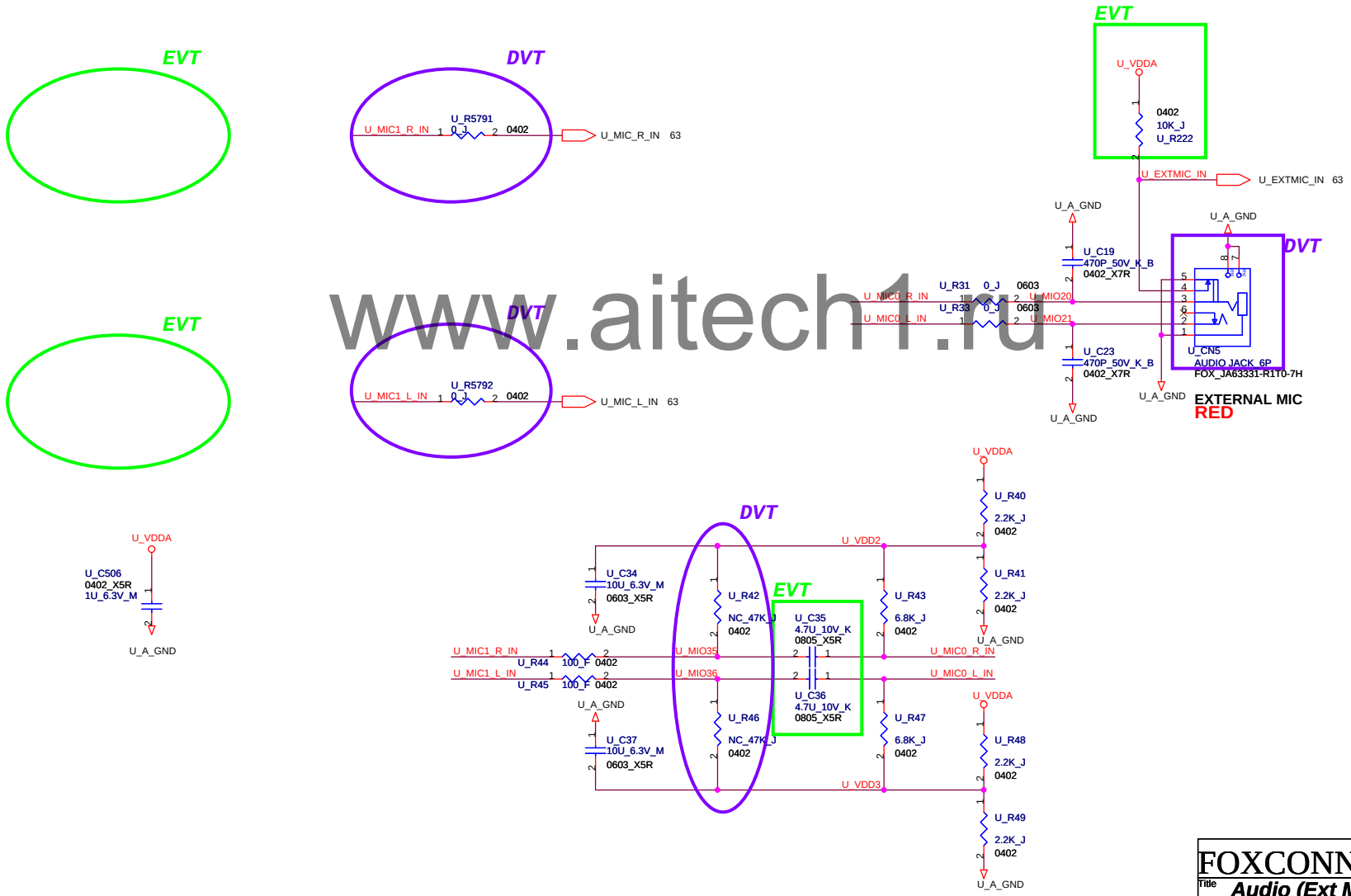
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	**Audio (Head Phone Jack)**	
Size A3	Document Number **M960&M970 H Model**	Rev **SA**
Date: Tuesday, December 29, 2009	Sheet 67 of 93	



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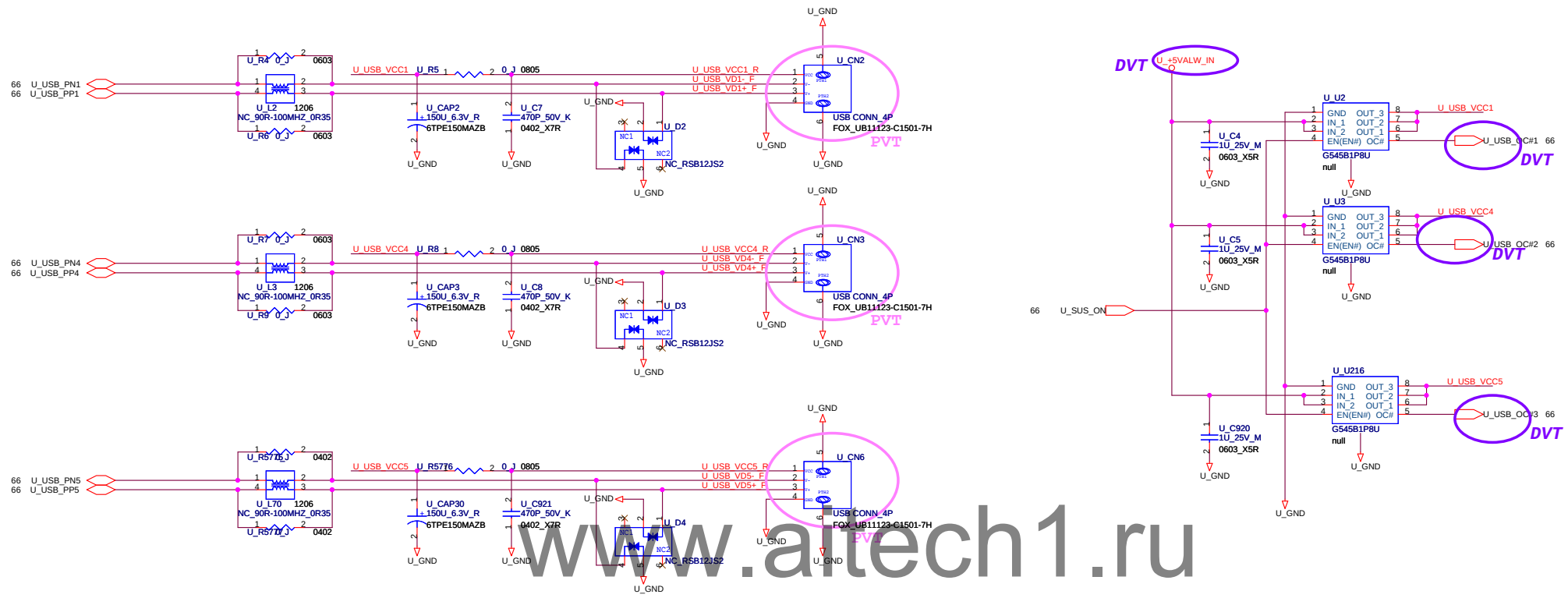
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (Ext MIC Jack)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 68 of 93	



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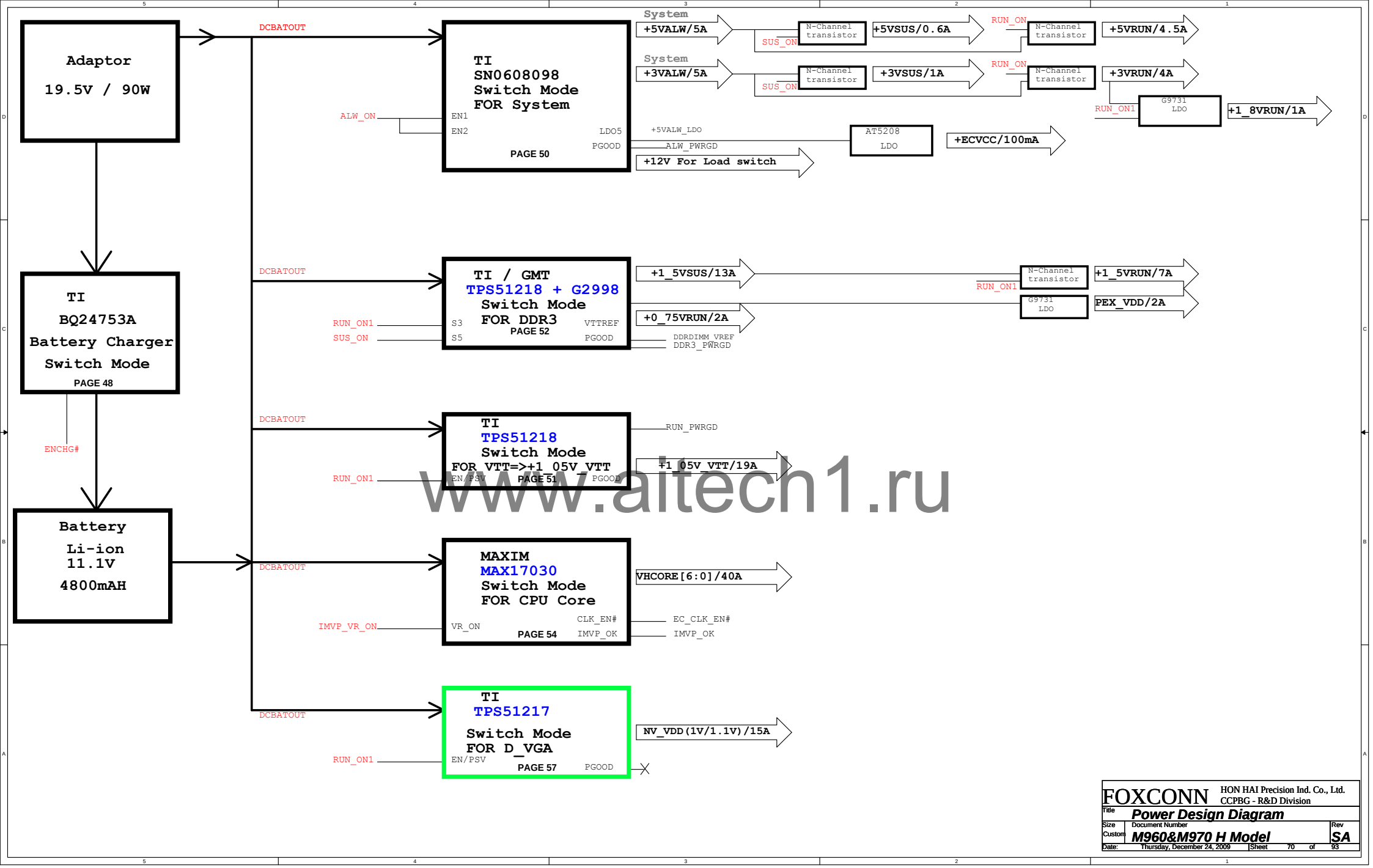
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (USB Port)	
Size: Custom	Document Number: M960&M970 H Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 69 of 93	



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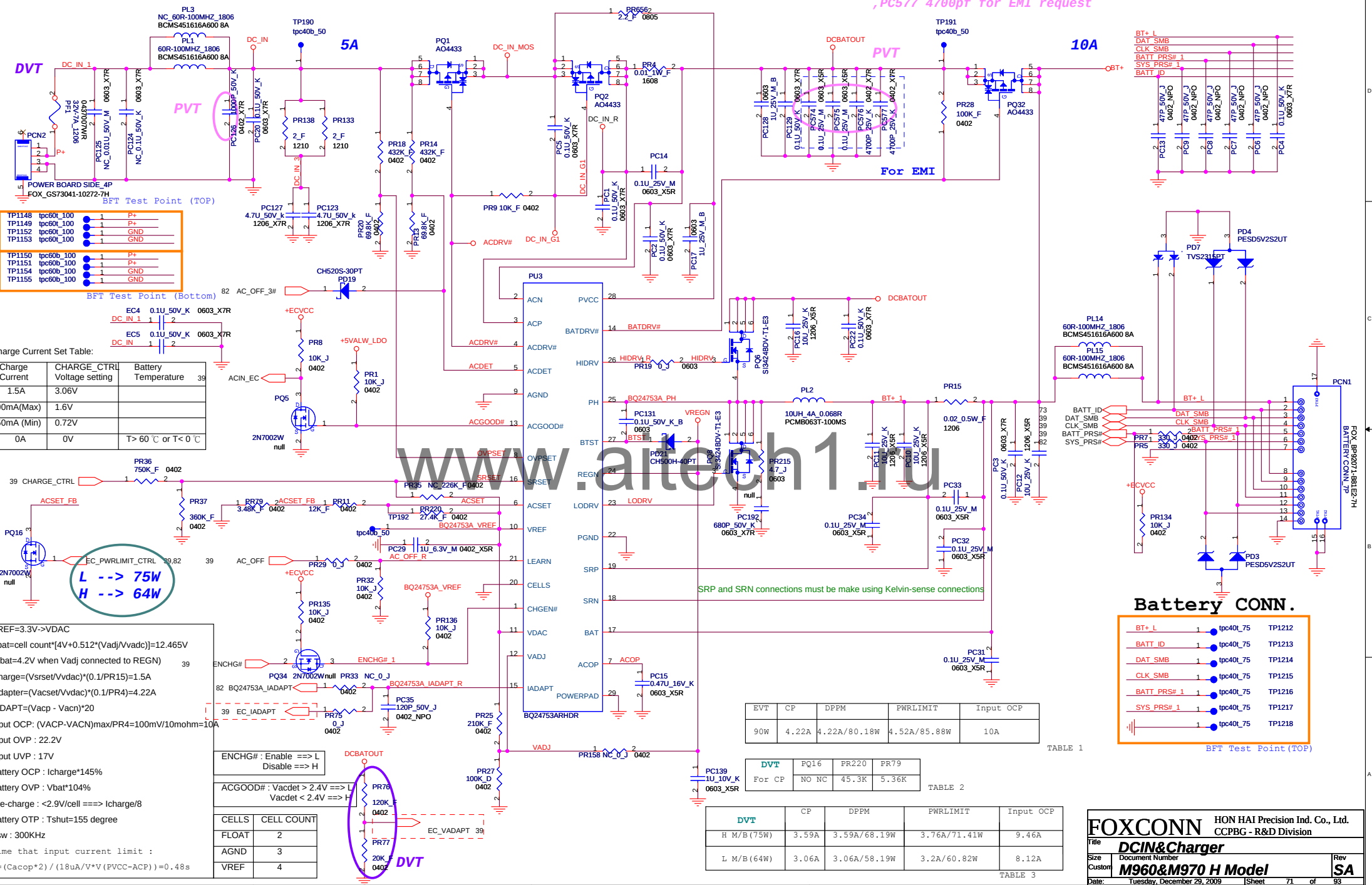
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Design Diagram	
Size: Custom	Document Number: M960&M970 H Model	Rev: SA
Date: Thursday, December 24, 2009	Sheet 70 of 93	

09/11/21 Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf ,PC577 4700pf for EMI request

ACP and ACN connections must be make using Kelvin-sense connections



Charge Current Set Table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
800mA(Max)	1.6V	
350mA (Min)	0.72V	
0A	0V	T> 60 ℃ or T< 0 ℃

VREF=3.3V->VDAC

Vbat=cell count*[4V+0.512*(Vadj/Vvadc)]=12.465V

(Vbat=4.2V when Vadj connected to REGN)

Icharge=(Vsrset/Vvdac)*(0.1/PR15)=1.5A

Iadapter=(Vacset/Vvdac)*(0.1/PR4)=4.22A

IADAPT=(Vacp - Vacn)*20

Input OCP: (VACP-VACN)max/PR4=100mV/10mohm=10A

Input OVP : 22.2V

Input UVP : 17V

Battery OCP : Icharge*145%

Battery OVP : Vbat*104%

Pre-charge : <2.9V/cell ===> Icharge/8

Battery OTP : Tshut=155 degree

Fsw : 300KHz

Time that input current limit :

t=(Cacop*2)/(18uA/V*V(PVCC-ACP))=0.48s

ENCHG# : Enable ==> L
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

EVT	CP	DPPM	PWRLIMIT	Input OCP
90W	4.22A	4.22A/80.18W	4.52A/85.88W	10A

TABLE 1

DVT	PQ16	PR220	PR79
For CP	NO NC	45.3K	5.36K

TABLE 2

DVT	CP	DPPM	PWRLIMIT	Input OCP
H M/B(75W)	3.59A	3.59A/68.19W	3.76A/71.41W	9.46A
L M/B(64W)	3.06A	3.06A/58.19W	3.2A/60.82W	8.12A

TABLE 3

www.altech1.ru

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: DCIN&Charger

Size: Custom | Document Number: M960&M970 H Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 71 of 93

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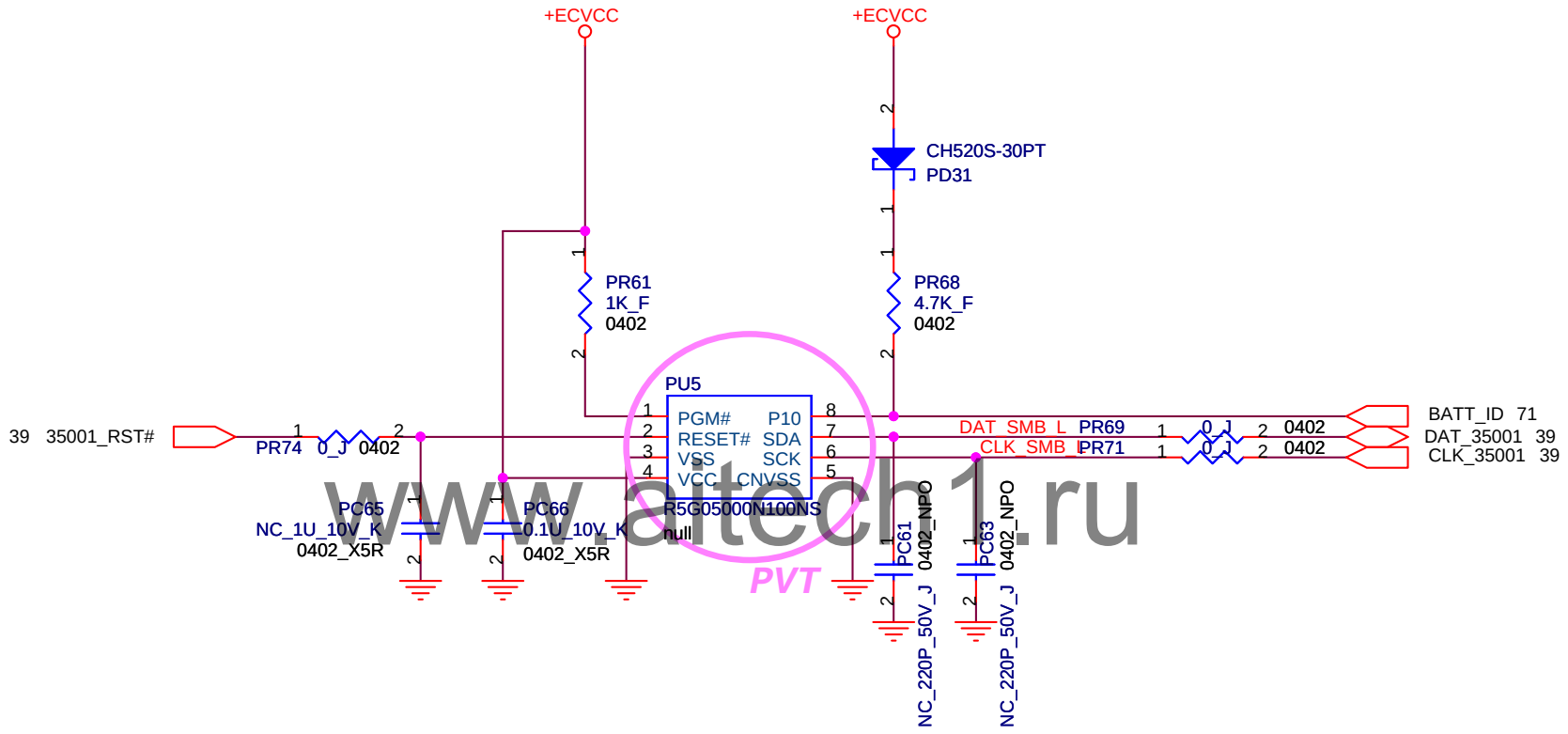
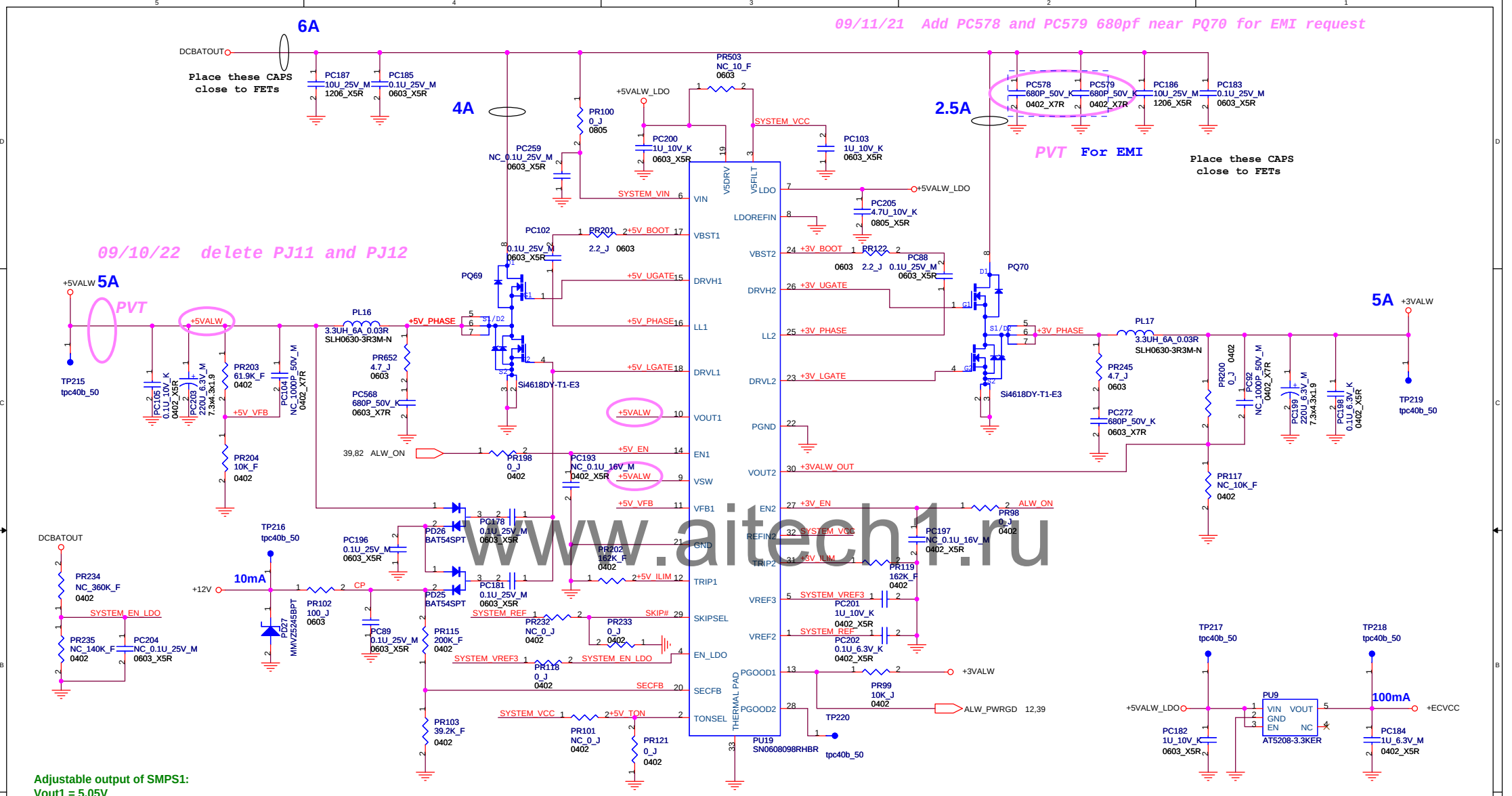
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**DISCHARGE CIRCUIT**	
Size A	Document Number **M960&M970 H Model**	Rev **SA**
Date: Thursday, December 24, 2009	Sheet 72 of 93	



www.altech1.ru
PVT

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***Identify IC***	
Size A	Document Number ***M960&M970 H Model***	Rev ***SA***
Date: Tuesday, December 29, 2009	Sheet 73 of 93	



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Adjustable output of SMPS1:
Vout1 = 5.05V
PR204 = 10K, PR203 = P204 x (Vout1 / 0.7V - 1) =61.9Kohm

Second Feedback :
Vout_sec = 12V, PR103 = 20Kohm
PR115 = PR103 x (Vout_sec / 2V - 1) =100Kohm

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

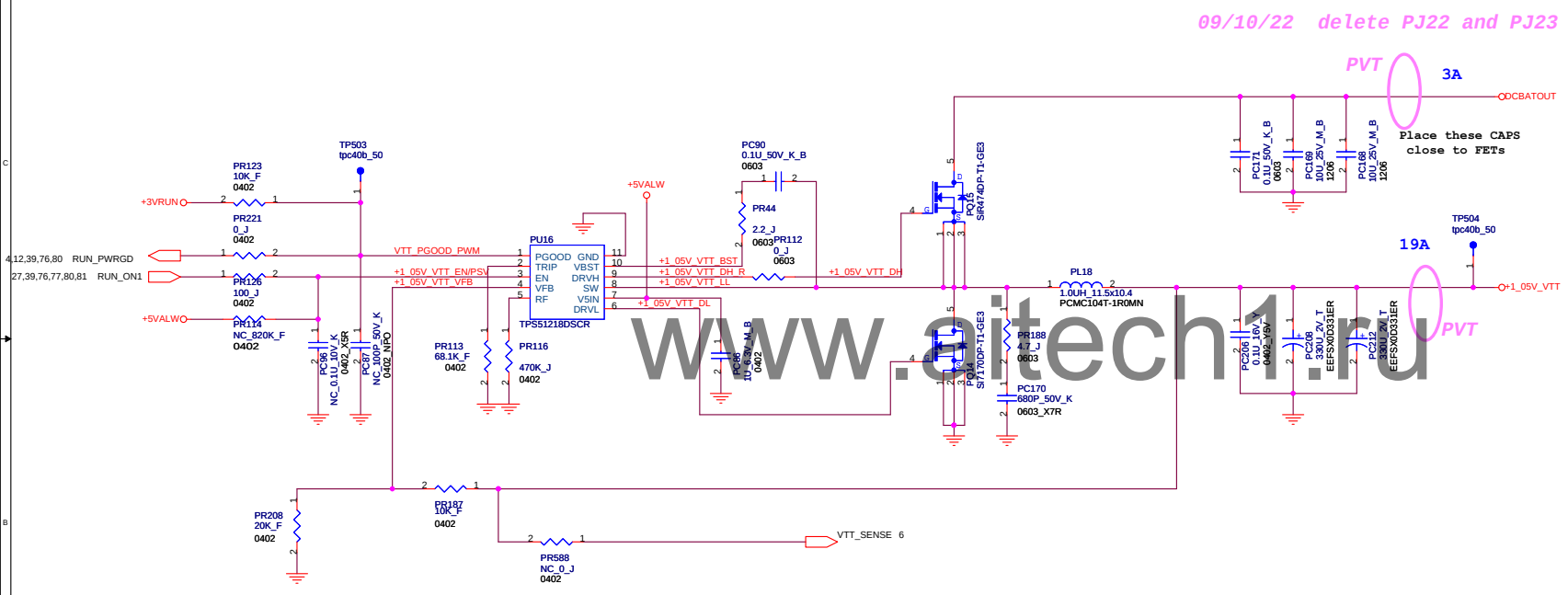
L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u
+5VALW=((PR186/PR188)+1)*VFB1

Current limit resistor for SMPS1 :
Ivalley_5 = 5.775A, Rcs_5 = Rds1 = 10.8mohm
PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

Current limit resistor for SMPS2 :
Ivalley_3 = 5.525A, Rcs_3 = Rds2 = 10.8mohm
PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	SYS Power (+3 3V/+5V)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 74 of 93	



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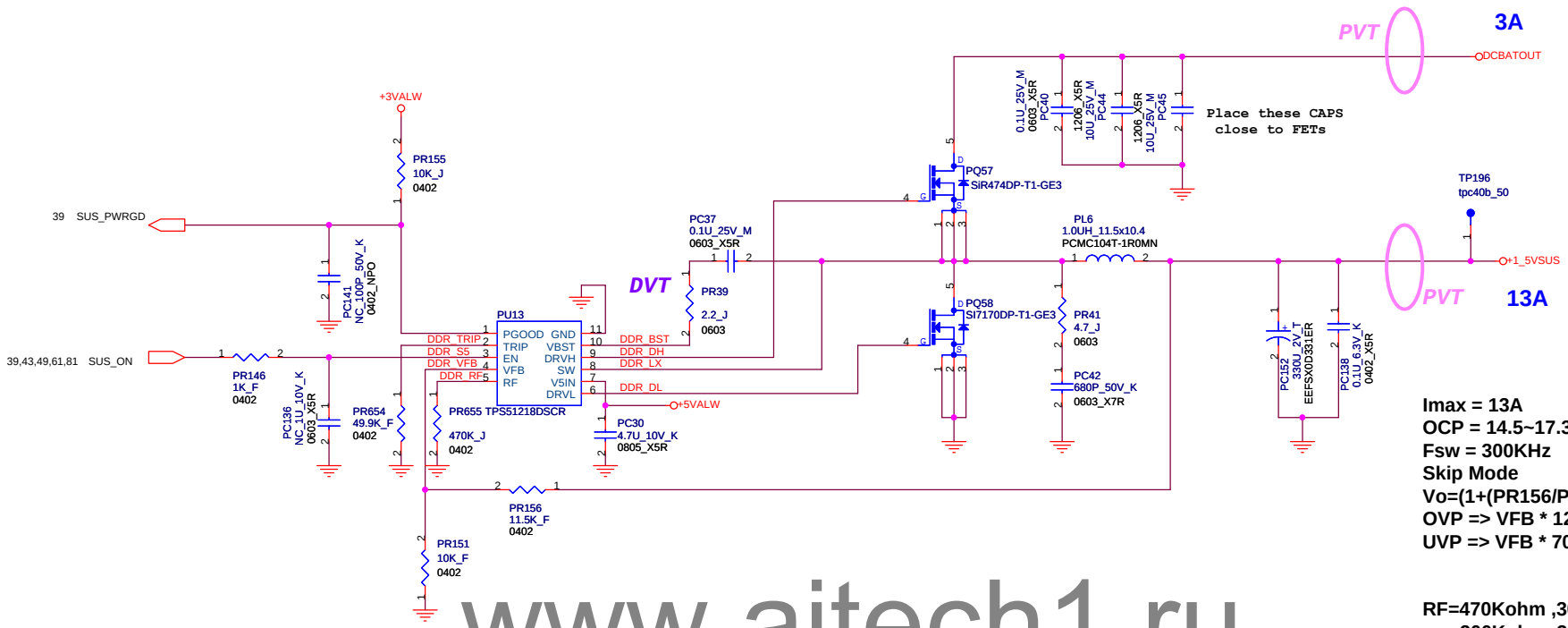
Imax = 19A
Fsw = 390KHz
Skip Mode
Vo=(1+(PR187/PR208))*0.704=1.05V
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_05V_VTT)	
Size Custom	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 75 of 93	

09/10/22 delete PJ26 and PJ27



Imax = 13A
OCP = 14.5~17.32A
Fsw = 300KHz
Skip Mode
Vo=(1+(PR156/PR151))*0.704=1.514V
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

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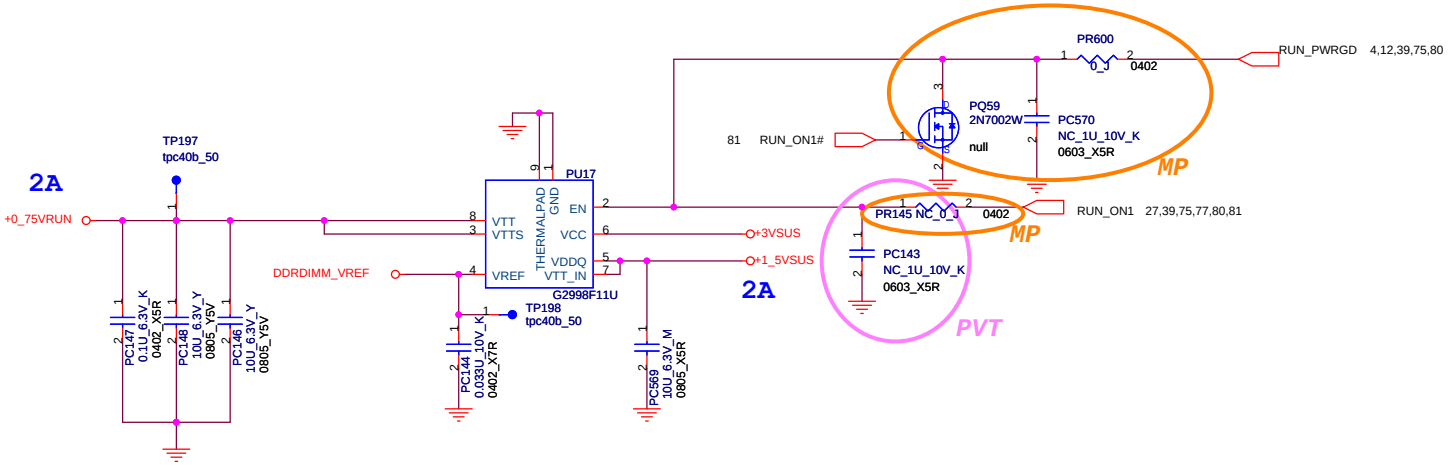
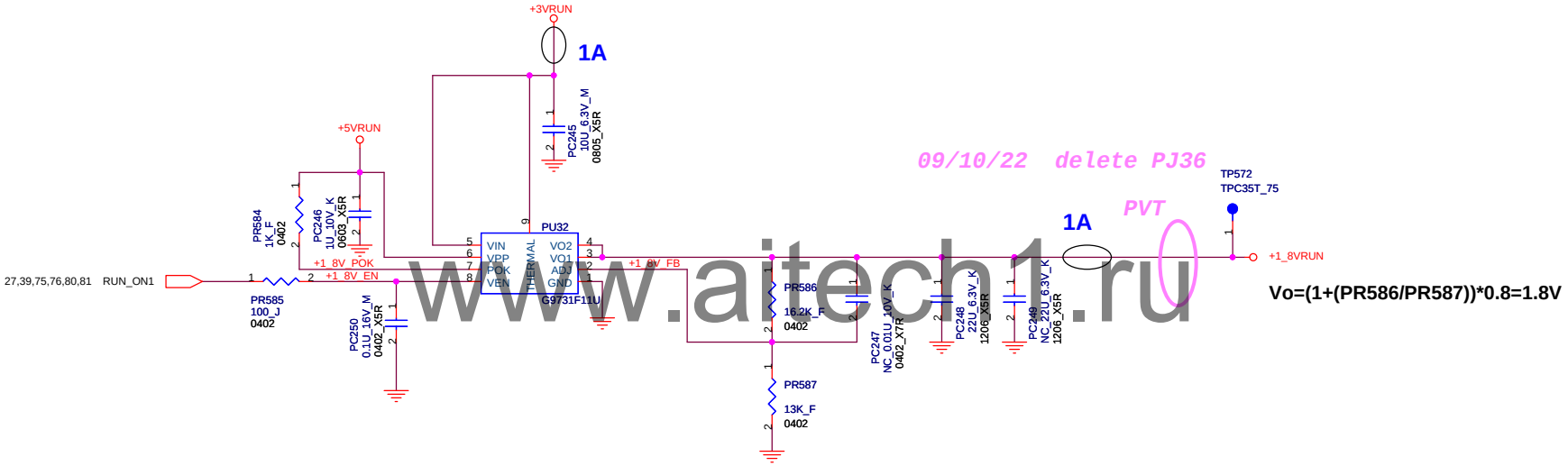


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR3 Power(+1_5V/+0_75V)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 76 of 93	



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FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_8V)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 77 of 93	

09/11/21 change PC151 and PC156 from NC to mount 0.1uf for EMI request

Placement TOP and BOTTOM Overlapped

Place these CAPS close to FETs

4A

DCBATOUT

PC110 10U_25V_M 1206_X5R
PC73 10U_25V_M 1206_X5R
PC151 0.1U_25V_M 0603_X5R
PC112 47U_25V_6.3x5.9 25SVPF47M

PVT

For EMI

PU28

MAX17030GTL+

PQ40 SIR428DP-T1-GE3

PQ38 SIR158DP-T1-GE3

PL8 0.36UH_28A_0.00076R ETQP4LR36AFC

PR555 2.21K_F 0402
PR556 NC_3.9K_F 0402
PR557 4.02K_F 0402
PR185 ERTJ1VR103J
PR594 2.2_F 0603
PC51 0.22U_25V_K 0603_X5R

PC244 330U_2V_7.3x4.3 EEFSX0D331XE
PC238 330U_2V_7.3x4.3 EEFSX0D331XE
PC229 330U_2V_7.3x4.3 EEFSX0D331XE
PC80 0.1U_6.3V_K 0402_X5R

TP507 tpc40b_50

40A

VHCORE

Placement TOP and BOTTOM Overlapped

Place these CAPS close to FETs

4A

DCBATOUT

PC111 10U_25V_M 1206_X5R
PC153 10U_25V_M 1206_X5R
PC156 0.1U_25V_M 0603_X5R

PVT

For EMI

PQ36 SIR428DP-T1-GE3

PQ37 SIR158DP-T1-GE3

PL5 0.36UH_28A_0.00076R ETQP4LR36AFC

PR569 2.21K_F 0402
PR572 NC_3.9K_F 0402
PR575 4.02K_F 0402
PR190 ERTJ1VR103J
PR596 2.2_F 0603
PC52 0.22U_25V_K 0603_X5R

PC241 330U_2V_7.3x4.3 EEFSX0D331XE
PC240 330U_2V_7.3x4.3 EEFSX0D331XE
PC77 0.1U_6.3V_K 0402_X5R

TP223 tpc40b_50

TP224 tpc40b_50

PR576 1K_J 0402

M8791_CSP3 PC278 NC_1000P_16V_K 0402_X7R

PR598 6.34K_F 0402
PR571 0_J 0402
PR573 NC_0_J 0402

PVT

PC253 1000P_50V_K 0402_X7R

PC254 NC_1000P_16V_K 0402_X7R

PC255 NC_1000P_16V_K 0402_X7R

PR519 0402 10_J

PR520 0_J 0402

VCCSENSE 6

VSSSENSE 6

Sense line are 18mil wide
Zo=27.4ohm

Valley current limit:
V_TIME_LIM = 0.2 x PR561 / (PR560 + PR561) = 22.54mV
I_LIM = V_TIME_LIM / Rcs = 21.26A

17030_IMON PR111 0_J 0402 IMVP_IMON 6

IMVP_PWRGD_PWM PR166 NC_0_J 0402 IMVP_PWRGD 12,39

TP224 tpc40b_50 PR127 0_J 0402 IMVP_OK 39

Rcs:
DCR = 0.76mohm
Rcs = DCR x (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.6061mohm

Load-Line R_FBAC: Loadl-Line=-1.9mV/A
Rcs = 0.709mohm
PR598 = (1.9mV/A) / (Rcs x 400us) = 6.34K

09/11/13 change pc253 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request

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FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	CPU Power VHCORE
Size A3	Document Number M960&M970 H Model
Rev	SA
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Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1

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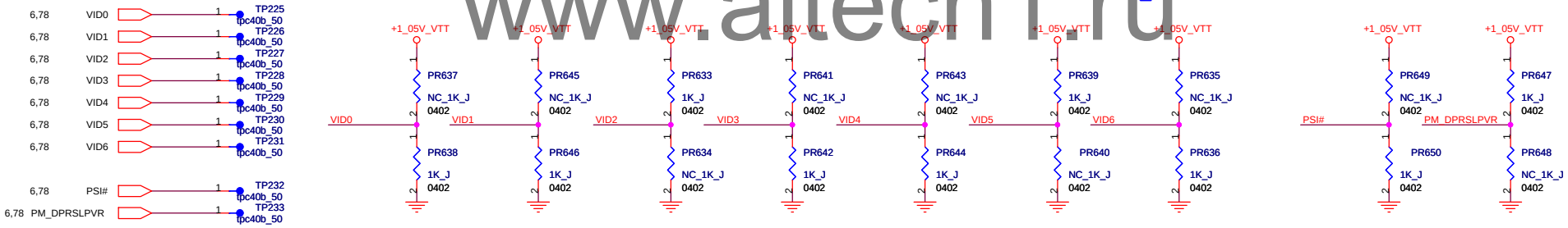
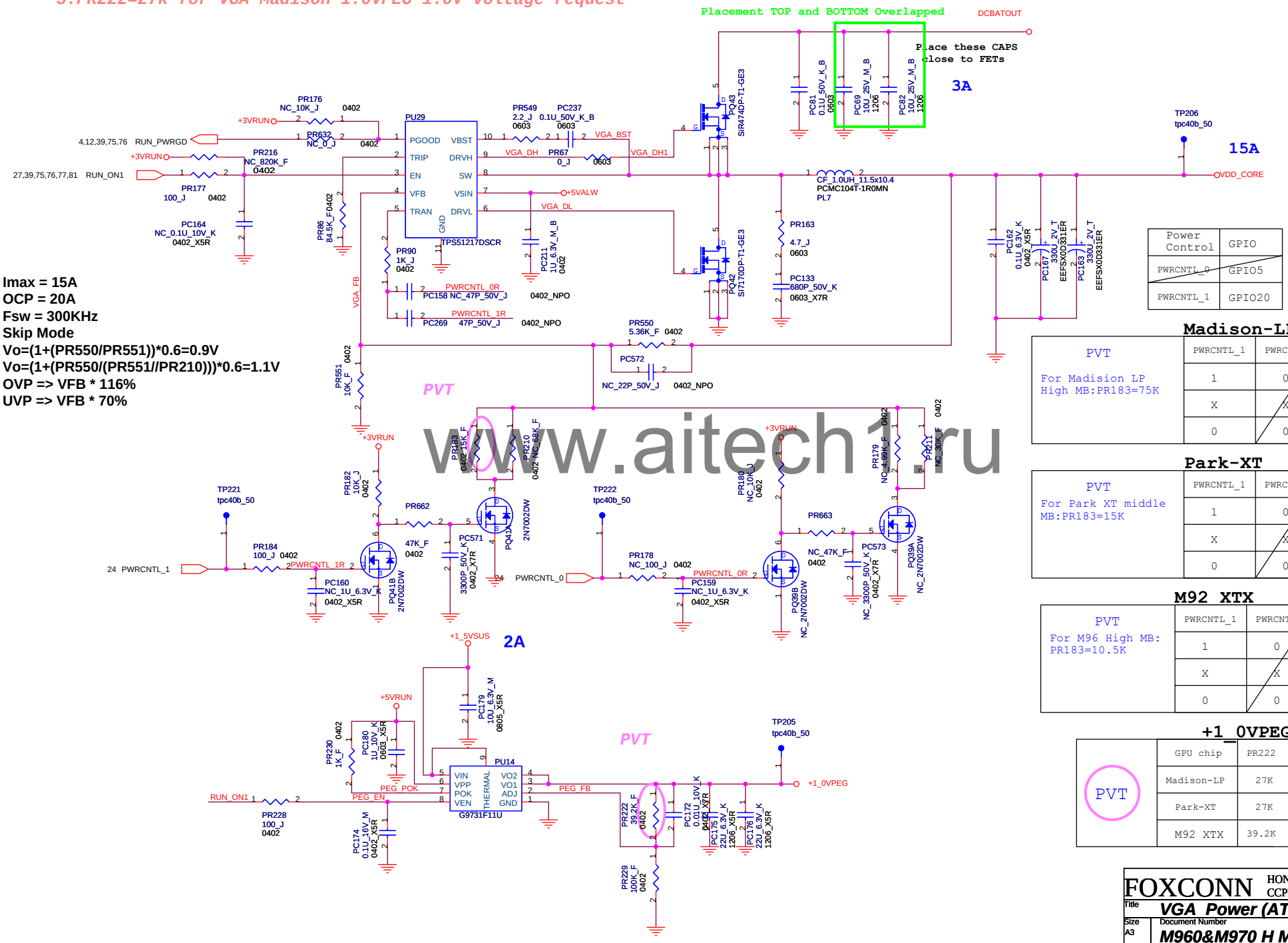


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CPU Power VID	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 79 of 93	

09/12/08 1.PR222=39.2k for VGA M92 XTX 1.0VPEG 1.1V voltage request
2.PR222=27k for VGA Park 1.0VPEG 1.0V voltage request
3.PR222=27k for VGA Madison 1.0VPEG 1.0V voltage request



Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO20

Madison-LP

PVT	PWRCNTL_1	PWRCNTL_0	GPU Voltage
For Madision LP High MB:PR183=75K	1	0	0.9V
	X	X	X
	0	0	0.95V

Park-XT

PVT	PWRCNTL_1	PWRCNTL_0	GPU Voltage
For Park XT middle MB:PR183=15K	1	0	0.9V
	X	X	X
	0	0	1.12V

M92 XTX

PVT	PWRCNTL_1	PWRCNTL_0	GPU Voltage
For M96 High MB: PR183=10.5K	1	0	0.9V
	X	X	X
	0	0	1.2V

+1_0VPEG

PVT	GPU chip	PR222	1_0VPEG voltage
	Madison-LP	27K	1.0V
	Park-XT	27K	1.0V
	M92 XTX	39.2K	1.1V

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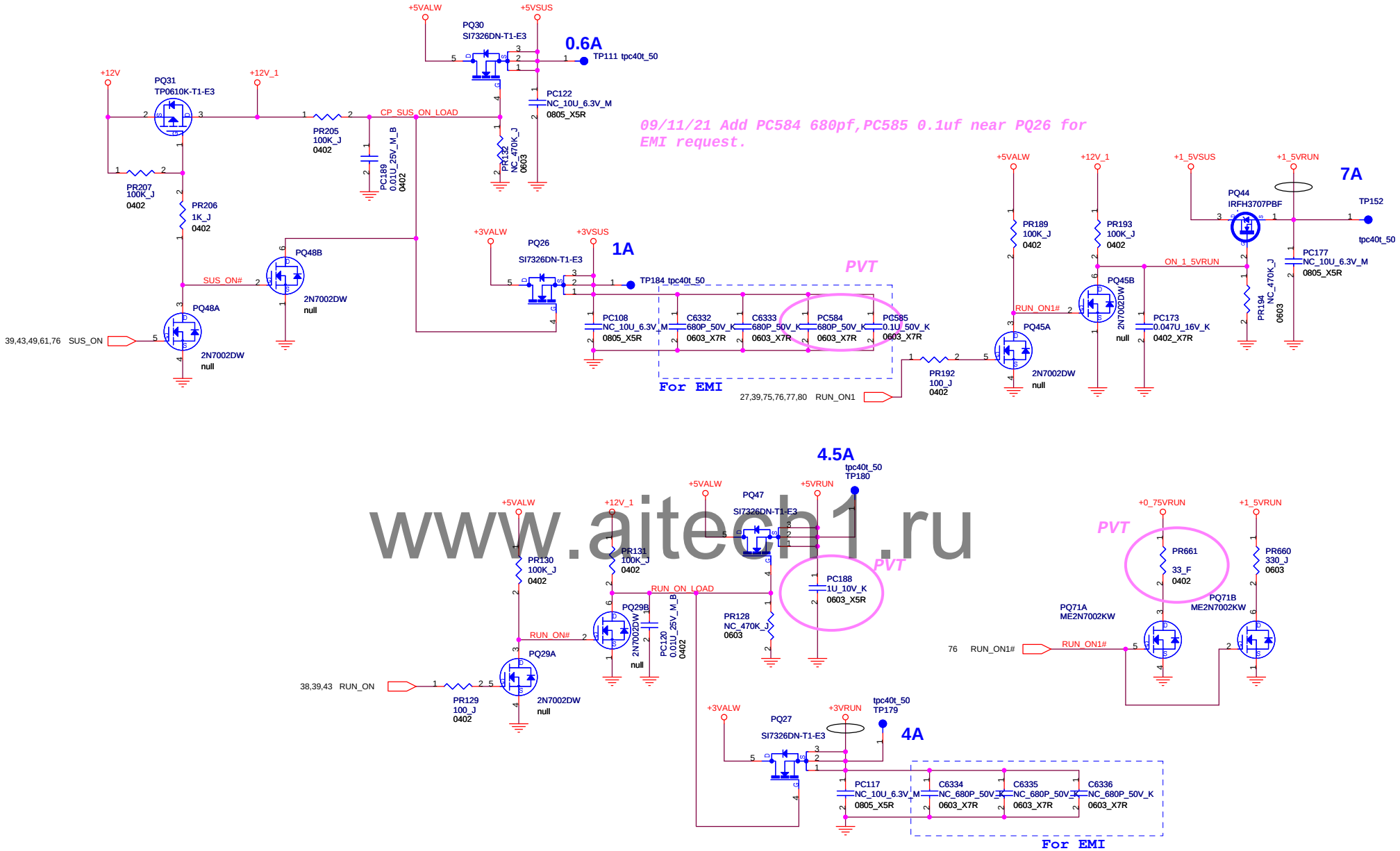
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA_Power (ATI_VDD)	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 80 of 93	



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FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size A3	Document Number M960&M970 H Model	Rev SA
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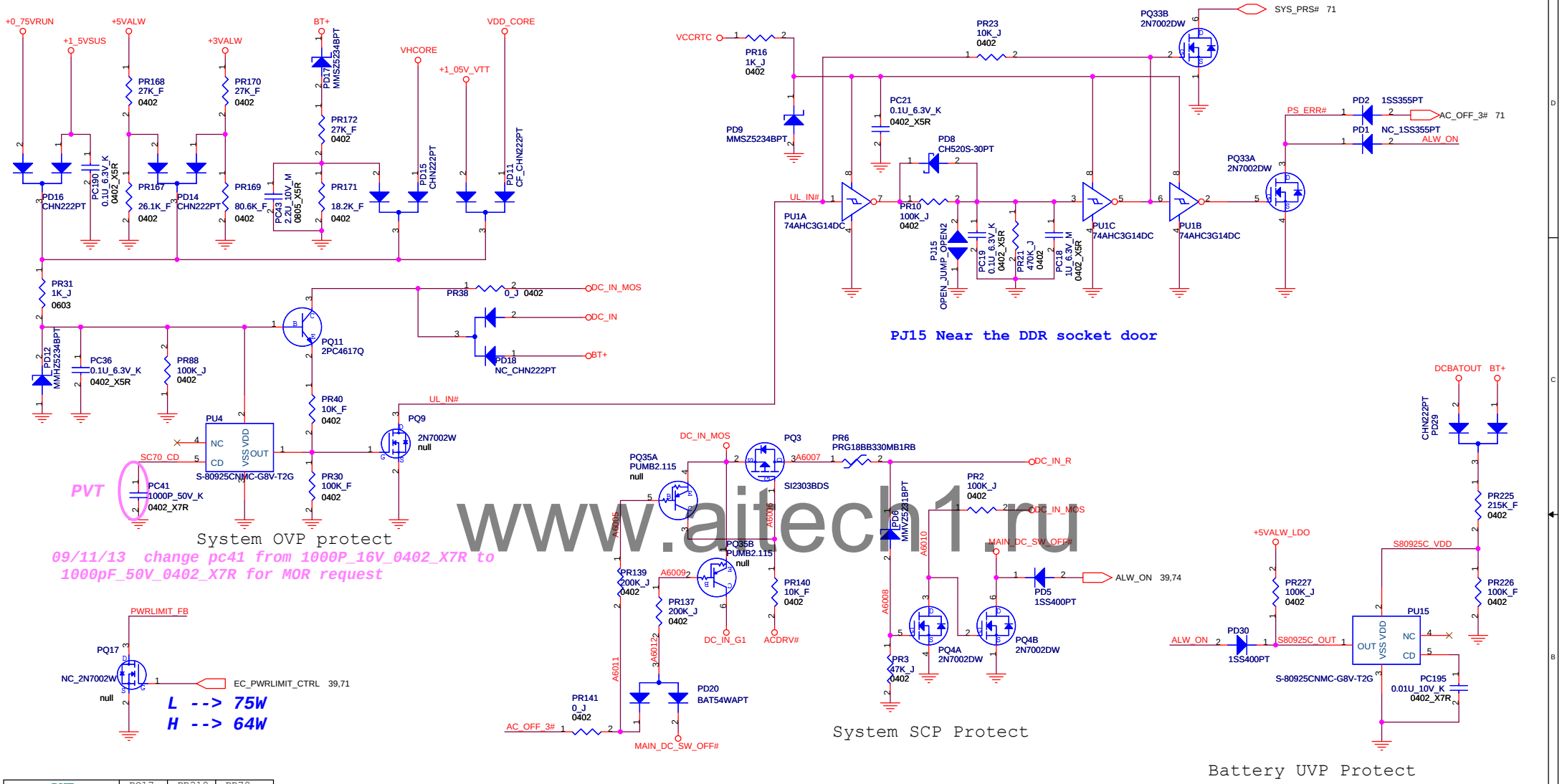

DVT	PQ17	PR218	PR78
For Power limit	NC	68.1K	2.05K

DVT	PWRLIMIT
H M/B(75W)	3.76A/71.41W
L M/B(64W)	3.2A/60.82W

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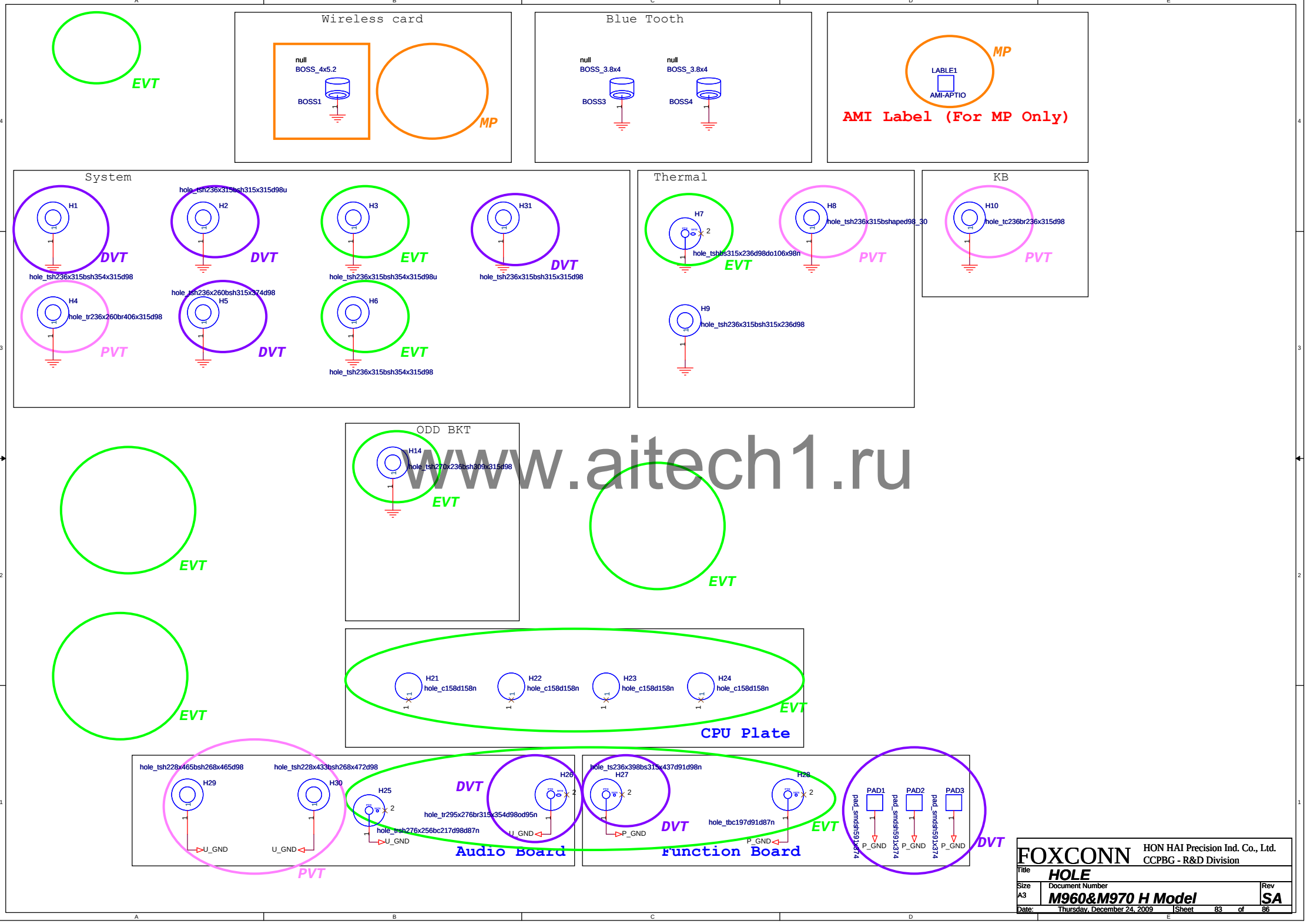
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: OVP protection

Size: A3 | Document Number: M960&M970 H Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 82 of 93



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FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE	
Size A3	Document Number M960&M970 H Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 83 of 86	

M960/M970 EVT

(2009/06/22)

P.25 [VGA(I/O)]Delete R5858 and R5859 for needless from AMD suggestion.
P.25 [VGA(I/O)]Connect VDD2DI to +1_8VRUN directly and delete.
P.28 L98,C[6254:6256] for AMD suggestion.
P.25 [VGA(I/O)]Connect A2VDD to +3V3_DELAY directly and delete.
P.28 L12,C529,C91,C85 for AMD suggestion.
P.28 [VGA(Power)]Delete net BIF_VDDC and C6156,C6157 for needless from AMD suggestion.
P.28 [VGA(Power)]Change VDD3 power plan from +1_8VRUN to +3V3_DELAY from AMD suggestion.
P.28 [VGA(Power)]Connect Ball AH29 to GND from AMD suggestion.
P.28 [VGA(Power)]The power for DPB can be shared with DPA from AMD suggestion.
P.28 [VGA(Power)]DPC and DPD can be powered directly without filters from AMD suggestion.
P.40 [EC]Add R5877,R5878 for SYSTEM_ID2 used from SW's requested.

(2009/06/23)

P.25 [VGA(I/O)]Delete R5846, R5847, R5848, R5849, R5838, R5839, R5840, C6188, C6189, U215 for needless from AMD suggestion.
P.73 [DCIN & Charger]Add test points TP1148~TP1155 for BFT test.
P.53 [Camera Connector]Add test points TP1156~TP1161 for BFT test.
P.57 [FAN]Add test points TP1162~TP1165 for BFT test.
P.35 [LAN]Add test points TP1166~TP1181 for BFT test.
P.43 [Debug Port]Add test points TP1186~TP1193 for BFT test.
P.61 [AUDIO Speaker Conn]Add test points TP1194~TP1197 for BFT test.
P.41 [KB Connector]Add test points TP1198~TP1207 for BFT test.
P.60 [SWITCH DB Conn.]Add test points TP1208~TP1211 for BFT test.
P.73 [DCIN&Charger]Add test points TP1212~TP1218 for BFT test.

P.41 [KB Connector]Del CN4 because M960 and M970 KB connectors are decided to co-use.
P.67 [AUDIO Speaker AMP]Del this page because AMP is combined with ALC275
P.39 [PCIE (MS&iLINK)]Change the net name from "SDMS_VCC" to "VCC_MS" because this net is for MS power only.
P.26 [VGA (Memory BUS) 4/6]Change the power source from +1_8VRUN to +1_5VRUN because the power source of DDR3 VRAM is +1_5VRUN.

(2009/06/24)

P.23 [CRT]Add and NC Q11,D9,R469,C279,R767,U9 for Semi-PNP.
P.39 [HDMI]Del C100,C107,C105,C106,C108,C109,C111,C112 for redundant design.
P.10 [PCH (HDA,JTAG,SAT)]Del R302 for redundant design.
P.24 [VGA (Strap) 2/6]Change net name "ATI_DVPDATA[23:20]" to ATI_DVPDATA[3:0] for AMD recommend.
P.24 [VGA (Strap) 2/6]Del R5767,R5768 for AMD recommend.
P.25 [VGA (I/O) 3/6]Del R5837 for AMD recommend.
P.26 [VGA (Memory BUS) 4/6]Add C6105,C6106,R5871,R5872 for AMD recommend.
P.13 [PCH (LVDS,DDI)]Del R1571 and place TP1219 on DDPD_HPD because this pin is not necessary for pull-low to GND.
P.55 [Felica Connector]Del F14,R5874,R5875 because the F14 related circuit is out of Felica spec.
P.55 [Felica Connector]Stuff C869,U48,R630,C845 because F14 related circuit is out of Felica spec.
P.72 [DCIN&CHARGE]Change DC-IN current form 8A to 5A.
P.72 [DCIN&CHARGE]Change PD7 from SMD15C to TVS2315PT.
P.74 [Idendify ID]Change PC61 from 1Uf_10V_k to 220Pf_50v_J,then NC PC61.
P.76 [VTT&PCH Power(+1_05V)]Change PR116 from 100k to 470k.
P.77 [DDR3 Power(+1_5V/+0_75V)]Change PR655 from 100k to 470k.
P.79 [CPU Power_VHCORE]Delete PC67,PC155.
P.82 [Other plane power]Change PQ29,PQ45,PQ48: from 2N7002DW to 2N7002SPT.
P.93 [OVP protection]Change PC41 from 0.01Uf to 1000Pf.

(2009/06/25)

P.45 [Mini-PCIE Card (WLAN)]Add R5901 on WLAN_EN for RF VEDS test.
P.23 [VGA (PCI-E) 1/6]NC R5831 for AMD M96.
P.26 [VGA (Memory BUS) 4/6]NC R5798,R5800,R5799,R5802,R5803,R5804 for AMD M96.
P.26 [VGA (Memory BUS) 4/6]NC R5779,R5880 for AMD M96.
P.28 [VGA (Power) 6/6]NC L90,C6196,C6194,C6195,C6192,C6193 for AMD M96.
P.28 [VGA (Power) 6/6]NC L91,C6197,C6194,C6199,C6200 for AMD M96.
P.28 [VGA (Power) 6/6]NC L26 for AMD M96.
P.28 [VGA (Power) 6/6]Add L30 and connect between VDD_CORE and SPV10 for AMD M96.
P.28 [VGA (Power) 6/6]NC L92,C6233,C6234,C6236 for AMD comment.
P.28 [VGA (Power) 6/6]NC L96,L97,C6248,C6251,C6249,C6252,C6250,C6253 for AMD comment.
P.26 [VGA (Memory BUS) 4/6]Change C6100 from 2200P to 1U for AMD comment.
P.28 [VGA (Power) 6/6]NC R5833,R5834 because M96 not support for PowerXpress.
P.28 [VGA (Power) 6/6]Add R587 and connect to GND for PowerXpress function of Park and Madison.
P.29 [VRAM(DDR3)# 1/4]Change R4030,R4019,R4027,R4028 from 1.33K to 4.99K for AMD comment.
P.29 [VRAM(DDR3)# 1/4]Add R5874,R5875,C6303 for AMD comment.
P.63 [SWITCH (Botton & KB LED)*]Change P_VR1,P_VR2,P_VR3,P_VR4,P_VR5 for EMC team request.
P.20 [DDRIII(SO-DIMM_0) 1/2]Del SPR1,J1.
P.20 [DDRIII(SO-DIMM_0) 1/2]Connect CN34 207 Pin to GND.
P.21 [DDRIII(SO-DIMM_0) 2/2]Connect CN35 G2 Pin to GND.

P.46 [LAN (88E8057) 1/2]Del R1462 for Marvell comment.
P.46 [LAN (88E8057) 1/2]NC C997,R94 for Marvell comment.
P.37 [Inverter Connector]Add U89C,R809,R684,C902,R772 for MOR's request.
P.37 [Inverter Connector]Change the off-page from "BL_OFF#" to "INV_EN" for MOR's request.
P.37 [Inverter Connector]Add U89A,U89B,C877,R687 for MOR's request.
P.37 [Inverter Connector]Add an off-page of BL_OFF# on U89D for MOR's request.
P.38 [LVDS Connector]Change the off-page of 35/36 pin of CN13 to INV_BRADJ/INV_ENABLE for MOR's request.
P.10 [PCH (HDA,JTAG,SAT)]Add R5905 to let JTAG_TCK pull down for MOR's request.
P.11 [PCH (PCI-E,SMBUS,CLK)]Add R539,R540 to let PCIECLKRQ3#,PCIECLKRQ4# to pull high to +3VRUN for MOR's request.
P.11 [PCH (PCI-E,SMBUS,CLK)]Add R579 to connect WLAN_CLKREQ# to +3VSUS for MOR's request.
P.11 [PCH (PCI-E,SMBUS,CLK)]NC R577 for MOR's request.
P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth function from port 13 to port10 to meet Freedom Project Product Specifications.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del GPIO39 related circuit because this pin is for LCDID3
P.51 [PCIE (MS&iLINK) 1/2]Delete i-Link function from Freedom_specV0.6.

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M960/M970 EVT

(2009/06/26)

P.19 [CLOCK GEN]Change U31 from SL28748ALC to SL28748CLC.
P.14 [PCH (PCI,USB,NVRAM)]Del USB_PN12,USB_PP12 off-page and add TP365,TP452 on tha same ports.
P.45 [Mini-PCIE Card (WLAN)]Del U45,C891 for disable WIMAX function
P.45 [Mini-PCIE Card (WLAN)]NC 36pin,38pin of CN12 for disable WIMAX function
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add an off-page "LCDID4" on GPIO48 and change the net name to LCDID4 for LCDID[4:0].
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del R5867 for LCDID[4:0].

P.63 [SWITCH (Botton & KB LED)*]Del "VAIO" button from Freedom Project Product Specifications V0.6.
P.63 [SWITCH (Botton & KB LED)*]Change the button names "Web" and "Display Off" to "Instant On" and "VAIO" from Freedom Project Product Specifications V0.6.
P.51 [PCIE (MS&iLINK) 1/2]Connect TPB+/- to GND and NC TPAP0/TPAN0/TPBIAS0 to disable i-Link function for Realtek comment.
P.51 [PCIE (MS&iLINK) 1/2]Add R1468 and NC it to disable i-Link function for Realtek comment.
P.12 [PCH (DMI,FDI,GPIO)]Connect SYS_PWROK line to ALW_PWRGD through D33 for MOR's request.

P.44 [Express Card]Add R5457 between the gate and the source of Q38 for MOR's request.
P.68 [AUDIO (Head Phone Jack)*]Add U_R220 pull-high to U_VDDA on U_HP_IN_5 for Realtek comment.
P.68 [AUDIO (Head Phone Jack)*]Change U_GND ground to U_A_GND for Realtek comment.
P.69 [AUDIO (Ext MIC Jack)*]Add U_R221 pull-high to U_VDDA on U_EXTMIC_IN for Realtek comment.
P.69 [AUDIO (Ext MIC Jack)*]Change U_C35/U_C36 to 4.7u X5R for Realtek comment.

P.84 [HOLE & AMI LABEL]Add H1~H20 for ME request.
P.25 [VGA (I/O) 3/6]Add 10K ohm resistors to let ATI_JTAG_TRSTB,ATI_JTAG_TDI, ATI_JTAG_TCLK,ATI_JTAG_TMS,ATI_JTAG_TDO pull up to +3V3_DELAY.

(2009/06/29)

P.68 [AUDIO (Head Phone Jack)*]Change U_A_GND which is connected to U_C9 pin2 to U_GND.
P.72 [DCIN&Charger]Change PCN1 connector to BP91071-B51E3-7H for ME request.
P.50 [eSATA Combo Conn.]Change CN27 connector to 3Q38111-R21C3-8H for ME request.
P.58 [Touch Pad]Change SW2/SW3/SW6/SW7 to 19-SKRPABE-1000 for ME request.
P.22 [Braidwood Connector]Change NC39 to 1N-0078002-F1G0 for ME request.
P.51 [PCIE (MS&iLINK) 1/2]Del R1468 and connect XOUT to U71 A2 for Ricoh's comment.

P.28 [VGA (Power) 6/6]NC AH29 U204E for AMD's comment.
P.16 [PCH (POWER) 1/2]Change R366,R325 to 100 ohm for Intel'comment.
P.16 [PCH (POWER) 1/2]Change C141 to 1U for Intel'comment.
P.09 [ARD (RESERVED)]Change R1274 to 3.3K for Intel's comment.

(2009/06/30)

P.25 [VGA (I/O) 3/6]Change JTAG_TCK to pull-low to GND through a 10K ohm resistor for MOR's request.
P.25 [VGA (I/O) 3/6]Del R5910 for MOR's request.
P.25 [VGA (I/O) 3/6]NC R5906,R5907,R5908,R5909 for MOR's request.
P.26 [VGA (Memory BUS) 4/6]Del C6105,C6106,R5879,R5880 for MOR's request.
P.28 [VGA (Power) 6/6]Del R5802,R5803 and connect DPE_VDD18/DPE_VDD10 to DPF_VDD18_[2:1]/DPF_VDD10_[2:1] for MOR's request.
P.28 [VGA (Power) 6/6]Del L96/C6248/C6249/C6250/L97/C6251/C6252/C6253 for MOR's request.
P.80 [CPU Power_VID]Stuff PR638,PR646 for Power request.
P.80 [CPU Power_VID]NC PR637,PR645 for Power request.
P.28 [VGA (Power) 6/6]Del L80/C859/C858/C860/L81/C862/C861/C6291/L82 /C6165/C6164/C866 for MOR's comment.

P.45 [Mini-PCIE Card (WLAN)]Del R824 for MOR's request.
P.12 [PCH (DMI,FDI,GPIO)]Change R911 to 10K for MOR's request.
P.54 [Bluetooth Connector]Del C378 for MOR's request.
P.28 [VGA (Power) 6/6]Del L6,Q7,Q9,R5828,R5829,R5830 because M960/M970 do not use BBP function.
P.45 [Mini-PCIE Card (WLAN)]NC CN12 15pin and del R18 for RF request.
P.56 [Status LED & LID]Add LED6/LED7/LED8/LED9 for M970 only.
P.45 [Mini-PCIE Card (WLAN)]Add R17 and NC it for MOR's request.

(2009/07/01)

P.25 [VGA (I/O) 3/6]Del TP1104,TP1105,TP1106,TP1230 because these test points are redundant.
P.28 [VGA (Power) 6/6]Change net name DPE_VDD18/DPE_VDD10 to DPEF_VDD18/DPEF_VDD10 for the co-use power DPE_VDD/DPF_VDD.
P.84 [HOLE & AMI LABEL]Del BOSS9,BOSS10 for ME request.
P.84 [HOLE & AMI LABEL]Add CPU hole H21,H22,H23,H24 for CPU socket.
P.50 [eSATA Combo Conn.]Del eSATA repeater schematic (U214,C766,C776,C759,C745, R5754,R5835,R5756,R5755,R5757,R5758,R5759,C718,C387) for over-design.
P.10 [PCH (HDA,JTAG,SAT)]Change SPI_CLK_SW/SPI_MOSI_SW/SPI_MISO_SW to SPI_CLK_L/SPI_MOSI_L/SPI_MISO_L for modifing the SW reserve design.
P.28 [VGA (Power) 6/6]Del R5833,R5834,R5837 and connect U204F AL21 to GND because M960/M970 do not have PowerXpress function.
P.25 [VGA (I/O) 3/6]Add two connection ATI_LVDS_SCL/ATI_LVDS_SDA to CN13 5/6 pin and pull-high 4.7K to +3V3_DELAY for SW request to add EDID function.

(2009/07/02)

P.38 [LVDS Connector]Connect CN13 Pin1 to LCDVCC for LCD power supply.
P.38 [LVDS Connector]Connect CN13 Pin34 to GND for LCD power supply.
P.51 [PCIE (MS&iLINK) 1/2]NC R820/C868/R817/C865/R818/C864 because SD_CD#/SD_WP#/MS_CD# has an internal pull-up resistor and the debouching circuit.
P.36 [LVDS]Update Panel ID and related information.

(2009/07/03)

P.10 [PCH (HDA,JTAG,SAT)]Del TP119/TP123/TP133/TP136/TP137/TP138 and R442 because this is SW reserve design.
P.14 [PCH (PCI,USB,NVRAM)]Del Q39/Q37/R5456/SW5/R300 for changing GNT1#/GNT0# control method.
P.14 [PCH (PCI,USB,NVRAM)]Add R345/R346 pull-high to +3VRUN for controling GNT1#/GNT0#.
P.14 [PCH (PCI,USB,NVRAM)]Change R344/R392/R345/R346 to 10K ohm.
P.45 [Mini-PCIE Card (WLAN)]Del R17 and change the net name "MINI_PCIE_+3_3V_R" to "MINI_PCIE_+3_3V" to del RF reserve circuit.
P.70 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 to 2N-0004009-MKG0 for ME request.

P.64 [AUDIO (CODEC)*]Change U_R5774 to 100K ohm and change the power source on it from U_VDDA to U_+12V because Gate voltage of U_Q55 is too low.
P.67 [AUDIO (AUDIO & USB Conn)*]Move U_SUS_ON to U_CN1 Pin22 and add U_+12V on Pin7.
P.62 [AUDIO/USB DB Conn.]Move SUS_ON to CN31 Pin29 and add +12V on Pin44.
P.37 [Inverter Connector]Del R400 for MOR's request.
P.38 [LVDS Connector]Add Q177/Q178/R5736/R5737/C575 and change L98 for rush current issue.
P.36 [LVDS]Del R136 for redundant design.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add a NC resistor R979 to let GPIO8 pull-low to GND.
P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth USB port to port13.
P.14 [PCH (PCI,USB,NVRAM)]Change USB External Port-1 to USB port5 and eSATA change to port0.

(2009/07/04)

P.45 [Mini-PCIE Card (WLAN)]Restore U45,C891 for WIMAX function.
P.45 [Mini-PCIE Card (WLAN)]Connect 36pin,38pin of CN12 to USB_PN12_L/USB_PP12_L for WIMAX function.
P.45 [Mini-PCIE Card (WLAN)]Add J5 to connect Pin42 and Pin44 of CN12 for MOR's request.

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(2009/07/07)

P.54 [Bluetooth Connector]Add C378 pull-low to GND refer to M930.
P.56 [Status LED & LID]Del POWER/SUSPEND LED and its related circuit for ID changing.
P.12 [PCH (DMI,FDI,GPIO)]Change R973 to 2.2K ohm for MOR's requirement.
P.28 [VGA (Power) 6/6]Add R5816 between GND to PX_EN and set N.C for MOR's request.
P.38 [LVDS Connector]Add Q177 and related RC for protecting rush current.
P.61 [AUDIO Speaker Conn]Del Q28/Q30/Q53 and connect Q25 and Q27 because short protection circuit can marge L channel and R channel.
P.04 [ARD (CLK,MISC,JTAG)]Add Q72 for Intel S3 Power Reduction issue.
P.72 [DCIN&Charger]Delete PR17.
P.75 [SYS Power (+3_3V/+5V)]Delete close_jump GP2.
P.77 [DDR3 Power(+1_5V/+0_75V)]Change 1.5VSUS full load from 12A to 13A.
P.77 [DDR3 Power(+1_5V/+0_75V)]Change PR654 from 46.4k to 49.9k
P.82 [Others power plane]Change 1.5VRUN full load form 6A to 7A.
P.82 [Others power plane]Add 1.5VRUN discharge circuit (add PR660 330ohm,PQ71 2N7002EPT).
P.38 [LVDS Connector]Del R474/R473 and related EDID circuit for disabling EDID.

(2009/07/08)

P.56 [Status LED & LID]Add Q18/Q21/Q48/Q51/R384/R390/R690/R691/R694/R695 for POWER/SUSPEND LED location changing.
P.54 [Bluetooth Connector]Del C378 because C377 has the same function.
P.40 [EC+KBC(NPCE783L)]Add SYSTEM_ID3 (R5891/R5900) for SKU control.
P.25 [LVDS Connector]NC CN13 Pin3 because EDID is disabled.
P.63 [SWITCH (Botton & KB LED)*]Del P_SW3 and add P_CN4 for POWER/SUSPEND LED location changing.
P.56 [Status LED & LID]Change Q18/Q21/Q50 to DTC114EUB for MOR's request.
P.07 [ARD (GRAPHICS POWER)]Change VDDQ power source from +1_5VSUS to +1_5VRUN for Intel S3 Power Reduction issue.
P.60 [SWITCH DB Conn.]Change CN2 to 14pin type for POWER/SUSPEND LED location changing.
P.63 [SWITCH (Botton & KB LED)*]Change P_CN3 to 14pin type for POWER/SUSPEND LED location changing.
P.51 [PCIE (MS&iLINK) 1/2]Change CN36 type for ME request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Set GPIO27 as RST_GATE for Intel S3 Power Reduction issue.
P.75 [SYS Power (+3_3V/+5V)]Change NC PR118 to NO NC PR118 and NC PR234,PR235.
P.83 [OVP protection]Delete reserved Power limit circuit(delete PU2,PU11,PD22 ,PR22,PR24,PR142,PR143,PR149,PR153,PR159,PR213,PR214,PC26,PC27,PC28).
P.83 [OVP protection]change PR218 from 37k to 45.3k.
P.11 [PCH (PCI-E,SMBUS,CLK)]Del R1590/R1591/R1592/Q73/Q74 and rename SMB_DATA_SB/SMB_CLK_SB to SMB_DATA_R/SMB_CLK_R.
P.10 [PCH (HDA,JTAG,SAT)]Del R1552/R1554 and rename SPI_CLK_L/SPI_MOSI_L to SPI0_CLK/SPI0_MOSI for redundant design.
P.10 [PCH (HDA,JTAG,SAT)]Add R5910 on SATA_LED# which is pull-high to +3VRUN for Intel comment.
P.04 [ARD (CLK,MISC,JTAG)]NC R1451/R1452 and stuff R1450/R1453 refer to M930.
P.52 [PCIE (SD) 2/2]Change CN29 type for ME request.
P.58 [Touch Pad]Change SW2/SW3/SW6/SW7 type for ME request.

(2009/07/09)

P.24 [VGA (Strap) 2/6]Change memory aperture size description for SW request.
P.68 [AUDIO (Head Phone Jack)*]Change Pin7/Pin8 of U_CN4 to U_A_GND for Layout request.
P.14 [PCH (PCI,USB,NVRAM)]Change USB_OC#5/USB_OC#4 to Pin7/Pin8 of RP18 for Layout request.
P.07 [ARD (GRAPHICS POWER)]Add a Open-Jump PJ43 between +1_5VRUN to VDDQ.
P.06 [ARD (POWER)]Del R856/R857 for MOR's request.
P.07 [ARD&CFD (GRAPHICS POWER)]Del R864/R866/R868/R869/R871 for MOR's request.
P.51 [PCIE (MS&iLINK) 1/2]Add damping resistors (R5911~R5919) on each MS signal.
P.52 [PCIE (SD) 2/2]Change C518/C522 to X5R type for MOR's request.
P.52 [PCIE (SD) 2/2]Add damping resistors (R5920~R5924) on each SD signal.
P.52 [PCIE (SD) 2/2]Change C767 to 10pF for MOR's request.
P.56 [Status LED & LID]Del LED7/LED8/LED10 for ME request.
P.38 [LVDS Connector]Add NC Cap. (C6306~C6313) between each LVDS differential lane.
P.46 [LAN (88E8057) 1/2]Modify R94/R97/C997 description.
P.46 [LAN (88E8057) 1/2]Change all resistors and caps to 88E8059 setting.
P.84 [HOLE & AMI LABEL]Add H25/H26/H27/H28 for ME request.
P.35 [CRT]Change CN20 type for ME request.
P.70 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 type for ME request.
P.84 [HOLE & AMI LABEL]Del H11/H12/H13/H15/H16/H17/H18/H19/H20 for ME request.
P.44 [Express Card]Rename PCIE_EXPRESS_WAKE# to PCIE_WAKE# to del reserve design.
P.12 [PCH (DMI,FDI,GPIO)]Del R290 and PCIE_EXPRESS_WAKE# off-page to del reserve design.
P.82 [Others power plane]Add 0.75V_RUN discharge circuit(add PR661 330ohm).
P.82 [Others power plane]Change PQ71 from 2N7002EPT to ME2N7002KW.
P.04 [ARD (CLK,MISC,JTAG)]Del the description of RST_GATE and add a 1k ohm resister R5925 between +1_5VSUS and DDR3_DRAMRST#.
P.04 [ARD (CLK,MISC,JTAG)]Add R5926/R5927/U217 for Intel S3 Power Reduction issue.
P.04 [ARD (CLK,MISC,JTAG)]Del R928/R929 and related description for Intel S3 Power Reduction issue.
P.53 [Camera Connector]Add R5928/R5929/C6314/C6315 For EMI verification.
P.37 [Inverter Connector]Add R5930 For EMI verification.

(2009/07/10)

P.22 [Braidwood Connector]Del P.22 and change the page number from 23~87 to 22~86 for removing Braidwood function.
P.14 [PCH (PCI,USB,NVRAM)]Del all Braidwood-related off-page for removing Braidwood function.
P.49 [eSATA Combo]Swap L62/L66/L67 for layout request.
P.62 [SWITCH (Botton & KB LED)*]Change the description "Instant On" to "Web(Instant On) for SW request".
P.50 [PCIE (MS&iLINK) 1/2]Del R820/C868/R817/C865/R818/C864 for Ricoh's FAE suggest.
P.50 [PCIE (MS&iLINK) 1/2]Add description of C794/C771/C774/C992 for Ricoh's FAE suggest.
P.50 [PCIE (MS&iLINK) 1/2]Add description of C790/C769/C770/C772/C799 for Ricoh's FAE suggest.
P.50 [PCIE (MS&iLINK) 1/2]Add description of C716/C717 for Ricoh's FAE suggest.
P.38 [HDMI]Connect Q57 D/S to +5VRUN_L188/+5VRUN_F.
P.37 [LVDS Connector]Connect Q177 D/S to DCBATOUT_L/DCBATOUT.
P.39 [EC+KBC(NPCE783L)]Change net name "KB_PRESENCE#" to "INST_ON_SW#" for SW request.
P.71 [DCIN&Charger]Delete NC PR12.
P.71 [DCIN&Charger]Change charge voltage form 12.48V to 12.465V for MOR request (change PR25 form 200k_F to 210K_F, change PR27 from 100K_F to 100K_D).
P.73 [Identify IC]Change PC66 from 0.1u_16v_0402_Y5V to 0.1u_10v_0402_X5R.
P.73 [Identify IC]Change NC PC65 1u_10v_0603_X5R to NC PC65 1u_10v_0402_X5R.
P.78 [CPU Power_VHCORE]Change PC112 from 100U_25V_M_Φ6.3*7.7mm to 68uF_25V_M_Φ6.3*5.8mm.

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(2009/07/11)

P.36 [Inverter Connector]Reverse CN5.
P.62 [SWITCH (Botton & KB LED)*]Reverse P_CN3.
P.37 [LVDS Connector]Add description on the circuit for inrush current issue of M870.
P.34 [CRT]Change F2 type for PUR request.
P.63 [AUDIO (CODEC)*]Change U_C459/U_C476/U_C787 type for PUR request.
P.07 [ARD (GRAPHICS POWER)]Add net name "+1_5VRUN_J".
P.14 [PCH (PCI,USB,NVRAM)]Del R344/R392 and the description about Boot-BIOS for SW request.
P.52 [Camera Connector]Add net name DMIC_CLK_R/DMIC_DAT_R and connect TP1160/TP1161 to the new net for TE request.
P.20 [DDRIII(SO-DIMM_0) 1/2]Reconnect SPR2/J2 to CN34 and CN35 for EMC request.
P.10 [PCH (HDA,JTAG,SAT)]Reverse CN26.
P.38 [HDMI]Change CN21 type for ME request.
P.60 [AUDIO Speaker Conn]Swap JSPK1 for ME request.

(2009/07/13)

P.51 [PCIE (SD) 2/2]Change U22 to G553E1P11U to meet MOR's request for SD.
P.57 [Touch Pad]Reverse CN8 for ME request.
P.62 [SWITCH (Botton & KB LED)*]NC P_VR2 for EMC reserve.
P.50 [PCIE (MS) 1/2]Del all i-Link related description.
P.36 [Inverter Connector]Reverse CN5.
P.83 [HOLE & AMI LABEL]Change H2/H3/H4/H5/H6/H7/H10/H14 type for ME request.
P.25 [VGA (Memory BUS) 4/6]Change C6100 type for PUR request.
P.71 [DCIN&Charger]Delete EC3 and C907.
P.79 [CPU Power_VHCORE]Change PC566 from 0.1U_6.3V_K to 0.1U_16V_K (HH PN:1C-2B20104-K300).
P.82 [OVP protection]Change PQ3 from IRLML5103TRPbF to SI2303BDS.
P.04 [ARD (CLK,MISC,JTAG)]Change U217 SUS_PWRGD to RUN_PWRGD.
P.63 [AUDIO (CODEC)*]Paste the schematic from P.48 of L model for MOR's request and Layout concern.
P.64 [AUDIO (MUTE)*]Paste the schematic from P.49 of L model for MOR's request and Layout concern.
P.65 [AUDIO (Power)*]Paste the schematic from P.50 of L model for MOR's request and Layout concern.
P.66 [AUDIO (AUDIO & USB Conn)*]Paste the schematic from P.51 of L model for MOR's request and Layout concern.
P.67 [AUDIO (Head Phone Jack)*]Paste the schematic from P.52 of L model for MOR's request and Layout concern.
P.68 [AUDIO (Ext MIC Jack)*]Paste the schematic from P.53 of L model for MOR's request and Layout concern.
P.69 [AUDIO (USB)*]Paste the schematic from P.54 of L model for MOR's request and Layout concern.
P.04 [ARD (CLK,MISC,JTAG)]Change R5926/R5927 to 1.5K/750 ohm for intel's comment.
P.81 [Others power plane]Change PR661 from 330ohm to 33ohm.

(2009/07/14)

P.38 [HDMI]Swap RP55/RP57/RP59/RP61 for Layout request.
P.49 [eSATA Combo]Swap L62/L66/L67 for Layout request.
P.37 [LVDS Connector]Swap Pin1 CN13 to Pin3 CN13 for cable design.
P.83 [HOLE & AMI LABEL]Change H4/H5/H7 footprint for ME request.
P.71 [DCIN&Charger]NC PR76 and PR77.
P.78 [CPU Power_VHCORE]Change PR555 and PR569 from 2.7K to 2.21K.
P.78 [CPU Power_VHCORE]NC PC260 ,NC PC261.
P.39 [EC+KBC(NPCE783L)]Pull-high INST_ON_SW# to +ECVCC for SW request.
P.76 [DDR3 Power(+1_5V/+0_75V)]Add PQ59(2N7002EPT)/PR600(100K)/PC570(1U_10V_K), then NC PQ59/PR600/PC570.

(2009/07/15)

P.48 [SATA CD-ROM]NC CN37 for ME request.
P.39 [EC+KBC(NPCE783L)]Del R5858 for redundant design.
p.78 [CPU Power_VHCORE]change PC112 from NOCHICON to Panasonic.
P.24 [VGA (I/O) 3/6]Connect GPIO_3/GPIO_4 to SMB_THRM_DATA/SMB_THRM_CLK for MOR's request.
P.09 [ARD (RESERVED)]Del RP83 and DQ_VREF off-page and add two test point to CPU for Intel's comment.
P.20 [DDRIII(SO-DIMM_0) 1/2]Del C35/C45/R1283 and DQ_VREF0 off-page for Intel's comment.
P.20 [DDRIII(SO-DIMM_0) 1/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
P.21 [DDRIII(SO-DIMM_1) 2/2]Del C37/C44/R1284 and DQ_VREF1 off-page for Intel's comment.
P.21 [DDRIII(SO-DIMM_1) 2/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
P.83 [HOLE & AMI LABEL]Add H29/H30/PAD1/PAD2/PAD3 for EMC request.
P.83 [HOLE & AMI LABEL]Change H28/H25 type for ME request.

(2009/07/16)

P.83 [HOLE & AMI LABEL]Change PAD1/PAD2/PAD3 for CIS request.
P.23 [VGA (Strap) 2/6]Modify description of VRAM.
P.20 [DDRIII(SO-DIMM_0) 1/2]Restore C35/C41 for MOR's request.
P.21 [DDRIII(SO-DIMM_1) 2/2]Restore C37/C44 for MOR's request.

(2009/07/17)

P.78 [CPU Power_VHCORE]Change PR565 from 10k to 1.8k, change PC566 from 0.1u to 0.022u.

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(2009/07/21)

p.1~88 [Page Data]Update all page data.

(2009/07/24)

P.84 [Braidwood Connector]Add CN39 and its related schematic for layout estimation.
P.14 [PCH (PCI,USB,NVRAM)]Add Braidwood related schematic for layout estimation.

(2009/07/30)

P.84 [Braidwood Connector]Del CN39 and its related schematic for layout estimation.
P.78 [CPU Power_VHCORE]Delete PJ42.
P.80 [VGA Power(ATI_VDD)]Delete PJ30, NC PR210, Change PR183 from 20K to 15.4K, Change PR550 from 2.7k to 5.36k.

(2009/08/13)

P.39 [EC+KBC(NPCE783L)]Del R5852 for OVT_EC# double pull-high.
P.13 [PCH (LVDS,DDI)]Change R223 from 0.5% to 5% for RGB disable guide.
P.60 [AUDIO Speaker Conn]Change JSPK1 to 1N-0004003-M1T0 for ME request.
P.66 [AUDIO (AUDIO & USB Conn)*]Reverse U_CN1 for moving U_CN1 from TOP to BOT side.
P.67 [AUDIO (Head Phone Jack)*]Changen U_CN4 to 2N-000600N-FKG0.
P.68 [AUDIO (Ext MIC Jack)*]Change U_CN5 to 2N-000600C-FRG0.
P.69 [AUDIO (USB)*]Change U_USB_OC#1/2/3 to U_USB_OC#0/2.
P.66 [AUDIO (AUDIO & USB Conn)*]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
P.61 [AUDIO/USB DB Conn.]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
P.14 [PCH (PCI,USB,NVRAM)]Del off-page USB_OC#1/3.
P.27 [VGA (Power) 6/6]Change Q77 to 17-2N7002W-0000 for PUR request.
P.04 [ARD (CLK,MISC,JTAG)]Change Q72 to 17-2N7002W-0000 for PUR request.
P.38 [HDMI]Change Q13 to 17-2N7002W-0000 for PUR request.
P.78 [CPU Power_VHCORE]Delete NC_PC260, NC_PC261.

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(2009/08/18)

P.34 [CRT]Change F2 to 0.35A.
P.83 [HOLE & AMI LABEL]Add H31 and change H1/H27/PAD1/PAD2/PAD3 for ME request.
P.49 [eSATA Combo]Swap CN27B.
P.43 [Express Card]Change R5457 to 470K and add NC R686 for MOR request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change RST_GATE from GPIO27 to GPIO46 , Stuff R982,NC R977.
P.46 [LAN (Transformer) 2/2]Change L70 for cost down.
P.51 [AUDIO (CODEC)*]Change U_U215.
P.25 [VGA (Memory BUS) 4/6]Change R5795,R5809,R5796,R5810 from 1R-000402X-F200 to 1R-0000101-F200 for vendor request.
P.27 [VGA (Power) 6/6]Stuff R5816 for vendor request.
P.24 [VGA (I/O) 3/6]Change R5793 from 1R-0000000-J200 to 1R-0000101-F200 and change R5794 from 1R-0000000-J200 to 1R-0000121-F200 for vendor request.
P.31 [VRAM(DDR3)# 4/4]NC R5727 for vendor request.
P.55 [Status LED & LID]Change U21 to 15-EC2648B-0000 for cost down.
P.71 [DCIN&Charger] Change PQ5,PQ16,PQ34 to 17-2N7002W-0000 for materials shortage.
P.76 [DDR3 Power(+1_5V/+0_75V)] Change PQ59 to 17-2N7002W-0000 for materials shortage.
P.82 [OVP protection] Change PQ9,PQ17 to 17-2N7002W-0000 for materials shortage.
P.81 [Others power plane] Change PQ29,PQ45,PQ48 to 17-2N7002D-W001 for materials shortage.
P.83 [HOLE & AMI LABEL]Change H29/H30 for ME request.

(2009/08/24)

P.69 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 for ME request.
P.60 [AUDIO Speaker Conn]Change JSPK1 for ME request.
P.34 [CRT]Change CN20 for ME request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R977 from NC to Stuff and change R982 from Stuff to NC.

(2009/08/25)

P.83 [HOLE & AMI LABEL]Change H26 for ME request.

(2009/08/27)

P.83 [HOLE & AMI LABEL]Change H30 for ME request.

(2009/08/31)

P.71 [DCIN&Charger]Change PCN1 to BP92071-B81E2-7H for ME request.
P.48 [SATA HDD]Change CN33 to LN21131-D40L-9H for ME request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add R5931/R5932/R5933/R5934 and change R5866 to 100K to pull-high LCDID for PE request.
P.35 [LVDS]Add R5935/R5936/R5937/R5938/R5939/R5940 to pull-low LCDID for PE request.

(2009/09/01)

P.56 [FAN]Del TP1163.
P.63 [AUDIO (CODEC)*]Add ALC269 co-lay schematic and del U_TP229, U_TP231, U_TP228.
P.14 [PCH (PCI,USB,NVRAM)]Del R1575 for redundant design (double pull-low).
P.64 [AUDIO (MUTE)*]Add ALC265 co-lay schematic.
P.10 [PCH (HDA,JTAG,SAT)]NC R5910 for redundant design (double pull-high).
P.74 [SYS Power (+3_3V/+5V)]Move TP215 from +5VALW_PWM to +5VALW for power test.
P.74 [SYS Power (+3_3V/+5V)]Move TP219 from +3VALW_PWM to +3VALW for power test.
P.75 [SYS Power(+1_05V_VTT)]Add TP504 for +1.05V_VTT power test.
P.78 [CPU Power_VHCORE]Add TP507,TP223,TP224 for VHCORE power test.
P.79 [CPU Power_VID]Add TP225~ TP233 for power test.
P.80 [VGA Power (ATI_VDD)]Change PR184 rome 1K to 100ohm, NC PC160 for vendor suggest.
P.80 [VGA Power (ATI_VDD)]Add TP221,TP222 for power test.
P.80 [VGA Power (ATI_VDD)]Add PR662 and PC571 for vendor suggest.
P.80 [VGA Power (ATI_VDD)]Add PC572(NC) for vendor suggest.

(2009/09/03)

P.25 [VGA (Memory BUS) 4/6]Stuff R5798, R5800, R5799, R5802, R5803, R5804 for Madison/Park only.
P.25 [VGA (Memory BUS) 4/6]Change R5806, R5807 to 0 ohm for Madison/Park only.
P.27 [VGA (Power) 6/6]Stuff L89,C6187,C6186,C6185 for Madison/Park only.
P.27 [VGA (Power) 6/6]Stuff R5811 for Madison/Park only.
P.22 [VGA (PCI-E) 1/6]Stuff R5831 for Madison/Park only.
P.27 [VGA (Power) 6/6]NC L76,L77,C6155,C6158 for Madison/Park only.
P.27 [VGA (Power) 6/6]Stuff L92, C6233, C6234, C6236, R5812 for Madison/Park only.
P.27 [VGA (Power) 6/6]Stuff L26, NC L30 for Madison/Park only.
P.27 [VGA (Power) 6/6]Stuff L90, C6192, C6193, C6194, C6195, C6196 for Madison/Park only.
P.27 [VGA (Power) 6/6]Stuff L91, C6197, C6199, C6200 for Madison/Park only.
P.27 [VGA (Power) 6/6]NC R5815 for Madison/Park only.
P.55 [Status LED & LID]Move R390/R384 to Drain side of Q51/Q48 for MOR comment.
P.37 [LVDS Connector]Change CN13 to M870 type (1N-0040000-FWG0).
P.59 [SWITCH DB Conn.]Change CN2 to 12pin type (1N-0012002-F0T0).
P.62 [SWITCH (Botton & KB LED)*]Change P_CN3 to 12pin type (1N-0012002-F0T0).
P.62 [SWITCH (Botton & KB LED)*]Move NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit to MB for MOR comment.
P.55 [Status LED & LID]Add NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit for MOR comment.
P.09 [ARD (RESERVED)]Del test points for MOR comment.
P.11 [PCH (PCI-E,SMBUS,CLK)]Del test points for MOR comment.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del test points for MOR comment.
Test Points[TP109/TP193/TP181/TP208/TP209/TP211/TP210/TP212/T213/TP214/TP235/TP236/TP265/TP266/TP237/TP239/TP327/TP328/TP329/TP256/TP257/TP259/TP260/TP262/TP263/TP264/TP284/TP287/TP288/TP289/TP290/TP291/TP292/TP293/TP294/TP295/TP296/TP297/TP298/TP425/TP1116/TP1117/TP1118/TP1119/TP140/TP147/TP148/TP149/TP148/TP145/TP144/TP134TP1120/TP1121/TP1122/TP1123/TP1124/TP188/TP183/TP88/TP91/TP93/TP101/TP412/TP416/TP415/TP417/TP414/TP421/TP422/TP423/TP424]
P.09 [ARD (RESERVED)]Del RP87 for MOR and Intel comment.
P.43 [Status LED & LID]Add LED test points TP1223/TP1224/TP1225/TP1226/TP1227/TP1228/TP1229/TP1230.
P.10 [PCH (HDA,JTAG,SAT)]Change U98 to W25Q32BVSSIG.
P.63 [AUDIO (CODEC)*]Del U_U7 and U_C155 for Realtek suggestion.
P.16 [PCH (POWER) 1/2]Del R897, R989 for MOR comment.
P.17 [PCH (POWER) 2/2]Del R428, R958 for MOR comment.
P.04 [ARD (CLK,MISC,JTAG)]Add R5950, C6316, R5951, R5949, R5948, C6317 for Intel S3 issue.

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(2009/09/08)

P.63 [AUDIO (CODEC)*]Change U_R327 to 1K.
P.71 [DCIN&Charger]NC PR33 for costdown.
P.80 [VGA Power (ATI_VDD)]Add PR663(NC) and PC573(NC) for vendor suggest.
P.82 [OVP protection]PR167 change to 26.1K, PR169 change to 80.6K , PR171 change to 18.2K for OVP Adjust
P.82 [OVP protection]Use SW PWRLIMIT function replaced HW PWRLIMIT circuit for costdown.(NC PU31,PC567,PR223,PR629,PR219,PR218,PR78,PC46.)
P.62 [SWITCH (Botton & KB LED)*]Change P_VR1/P_VR2/P_VR3/P_VR4 to 19-MLVS060-5000.
P.39 [EC+KBC(NPCE783L)]Change C27/C26 to 15p for Crystal vendor comment.
P.10 [PCH (HDA,JTAG,SAT)]Change C727/C702 to 15p for Crystal vendor comment.
P.50 [PCIE (MS) 1/2]Change C785/C786 to 22p for Crystal vendor comment.
P.49 [eSATA Combo Conn.]Add eSATA reperater schematic and NC it.
P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to GB5RF120-1203-7F for Halgen Free.
P.42 [Debug Port]Change CN30 to GB5RF120-1203-7F for Halgen Free.
P.54 [Felica Connector]Add Felica power supply schematic as Pokerman type for MOR request.
P.14 [PCH (PCI,USB,NVRAM)]Change USB_OC# signal to EVT type for MOR request.
P.41 [SPI Flash ROM]Change U23 to W25X10BVSNIG for SW comment.
P.63 [AUDIO (CODEC)*]Move U_R5774 to P.60 and rename to R5968.
P.61 [AUDIO/USB DB Conn.]NC +12V and add a +5VALW pin for USB VEVS test.
P.66 [AUDIO (AUDIO & USB Conn)*]NC U_+12V to a U_+5VALW pin for USB VEVS test.
P.61 [AUDIO/USB DB Conn.]Change CN31 to 1N-0050004-F0T0 for ME request.
P.66 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 to 1N-0050004-F0T0 for ME request.
P.45 [LAN (88E8057) 1/2]Add R5965/R5966/R5967 for 88E8057/88E8059 co-lay.
P.61 [AUDIO/USB DB Conn.]Change CN31 Pin 43 to GND.
P.66 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 Pin 43 to GND.
P.55 [Status LED & LID]Change Q49/Q179/Q180/Q181 to 17-DTA114Y-UB00 for PUR suggest.
P.44 [Mini-PCIE Card (WLAN)]Change Q5 to 17-DTC144E-UB00 for PUR suggest.
P.56 [FAN]Change Q80 to 17-DTC144E-UB00 for PUR suggest.
P.71 [DCIN&Charger]Change TP1148,TP1149,TP1150,TP1151 from DC_IN_1 to P+ for power test.
P.71 [DCIN&Charger]Change PQ16,PR76,PR77 from NC to mount for EC PWRLIMIT function.
P.71 [DCIN&Charger]Change PR79 from 0 to 3.48K, change PR11 from 20K to 12K for EC PWRLIMIT function.
P.73 [Identify IC]Add PD31 and change PR68 from 10K to 4.7K for MOR side request.
P.81 [Others power plan]Delete TP189,TP203 for power test.

(2009/09/09)

P.42 [Debug Port]Del TP1186~TP1193.
P.24 [VGA (I/O) 3/6]Add ATI_LVDS_SCL/ATI_LVDS_SDA for EDID function.
P.37 [LVDS Connector]Add ATI_LVDS_SCL/ATI_LVDS_SDA for EDID function.
P.74 [SYS Power (+3_3V/+5V)]Change PR652,PR245 from NC to mount 4.7ohm. Change PC568,PC272 from NC to mount 680pF for EMI suggest.
P.75 [SYS Power(+1_05V_VTT)]Change PR188 from NC to mount 4.7ohm, Change PC170 from NC to 680pF for EMI suggest.
P.76 [DDR3 Power(+1_5V/+0_75V)]Change PR41 from NC to mount 4.7ohm, Change PC42 from NC to mount 680pF for EMI suggest.
P.80 [VGA Power (ATI_VDD)]Change PR163 from NC to mount 4.7ohm, Change PC133 from NC to mount 680pF for EMI suggest.
P.52 [Camera Connector]Del R5928/R5929 and add L93/L94 for EMC request for DMIC noise.
P.52 [Camera Connector]Mount C6314/C6315 for EMC request for DMIC noise.
P.60 [AUDIO Speaker Conn]Del R5870, R5871, R5872, R5873 and Add L95, L96, L97, L98 for EMC request to filtrate SPK noise.
P.37 [LVDS Connector]Add C6324/C6325 for EMC request for 150MHz powerbase issue.
P.42 [Felica Connector]Change Felica power supply from +5VSUS to +3VSUS.
P.51 [PCIE (SD) 2/2]Change R391 to 100K for MOR request.
P.43 [Express Card]NC Q38, R5457 and mount R686 for MOR comment.

(2009/09/10)

P.37 [LVDS Connector]Add CN13 Pin40 for EDID function.
P.44 [Mini-PCIE Card (WLAN)]Add C6329/C6330 for EMI request.
P.16 [PCH (POWER) 1/2]Add C6326/C6327/C6328 for EMI request.
P.62 [SWITCH (Botton & KB LED)*]Change P_LED1/P_LED2/P_LED3 to HT-170UYG.
P.81 [Others power plane]Add C6332/C6333 on +3VSUS for EMI request.
P.81 [Others power plane]Add C6334/C6335/C6336 on +3VRUN for EMI request.
P.45 [LAN (88E8059) 1/2]Del R97 and add C6341 for Marvell FAE request.
P.45 [LAN (88E8059) 1/2]Del R5966, R5967 for Marvell FAE request.
P.45 [LAN (88E8059) 1/2]Change C993 to 10u for Marvell FAE request.
P.43 [Express Card]Correct Express Card SPEC.
P.48 [SATA CD-ROM]Del CN37 for MOR request.
P.61 [AUDIO/USB DB Conn.]Add F1 for MOR comment.
P.66 [AUDIO (AUDIO & USB Conn)*]rename U_+5VALW to U_+5VALW_IN for MOR comment.
P.69 [AUDIO (USB)*]Del U_F1 and rename U_+5VALW to U_+5VALW_IN for MOR comment.
P.83 [HOLE & AMI LABEL]Del BOSS2 for MOR request.
P.63 [AUDIO (CODEC)*]Change U_R321 to 100K for MOR request.
P.64 [AUDIO (MUTE)*]NC U_C472 for MOR comment.
P.68 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
P.68 [AUDIO (Ext MIC Jack)*]Del U_C26, U_C31 and add U_R5791, U_R5792 for MOR comment.
P.68 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
P.63 [AUDIO (CODEC)*]NC U_C923.
P.67 [AUDIO (Head Phone Jack)*]Change U_GND to U_A_GND for Realtek FAE suggest.
P.37 [LVDS Connector]NC CN13 Pin7.

(2009/09/11)

P.71 [DCIN&Charger]Change PR15 to RLM12FTSR020 for PUR request.
P.71 [DCIN&Charger]Change PF1 to 0437007.WR for PUR request.
P.37 [LVDS Connector]Change CN13 for Halgen-free.
P.60 [AUDIO Speaker Conn]Swap JSPK1 for layout concern.
P.44 [Mini-PCIE Card (WLAN)]Change SW4 to 1BS007-12110-002-7H for ME request.
P.55 [Status LED & LID]Change LED3/LED4 vendor to Everlight.
P.67 [AUDIO (Head Phone Jack)*]Change U_A_GND to U_GND for Realtek FAE suggest.
P.63 [PCIE (SD) 2/2]Change CN29 to WK21923-S6P3-4H for ME request.
P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to No Halgen-free.
P.42 [Debug Port]Change CN30 No Halgen-free.
P.62 [SWITCH (Botton & KB LED)*]Change P_CN3 to No Halgen-free.
P.59 [SWITCH DB Conn.]Change CN2 to No Halgen-free.
P.56 [FAN]Change CN14 to No Halgen-free.
P.60 [AUDIO Speaker Conn]Change JSPK1 to No Halgen-free.
P.83 [HOLE & AMI LABEL]Change H2/H4/H5 for ME request.
P.39 [EC+KBC(NPCE783L)]NC U216 Pin8 and del R575.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect DIS_FAN_MON# to U69F GPIO57 and pull-high to +3VRUN.
P.39 [EC+KBC(NPCE783L)]NC U4A Pin20 and add SYSTEM_ID1 off-page.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID1 to U69F GPIO17 and del R965.
P.39 [EC+KBC(NPCE783L)]NC U4A Pin27 and add SYSTEM_ID0 off-page.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID0 to U69F GPIO16 and NC RP19 Pin7.
P.39 [EC+KBC(NPCE783L)]NC U216 Pin9.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect PM_SLP_ME# to U4B GPIO26.
P.39 [EC+KBC(NPCE783L)]Del R5853 and connect INST_ON_SW# to GPIO12.
P.39 [EC+KBC(NPCE783L)]NC U216 Pin3 and connect WLAN_EN to U4A Pin20.
P.39 [EC+KBC(NPCE783L)]NC U216 Pin4 and connect BT_ON to U4A Pin27.

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(2009/09/11)

P.39 [EC+KBC(NPCE783L)]NC U216 Pin5/Pin6 and connect AC_OFF/EC_PWRLIMIT_CTRL to U4A Pin119/Pin120.
P.39 [EC+KBC(NPCE783L)]Del R5855/R5856/C6201/C6202.
P.39 [EC+KBC(NPCE783L)]Connect AC_Present to U4A Pin124.
P.39 [EC+KBC(NPCE783L)]Del U216/R5857/C6203.
P.25 [VGA (Memory BUS) 4/6]Change C6100 to UMK105CH680KW-F for PUR request.
P.34 [CRT]Del F2 for MOR comment.
P.63 [AUDIO (CODEC)*]Del U_R5773/U_Q64/U_R5771/U_R5783/U_U215/U_R5784 for MOR comment.
P.63 [AUDIO (CODEC)*]Move U_AMP_PD# to U_U18 Pin4.
P.64 [AUDIO (MUTE)*]Mount U_R352/U_R351/U_Q17/U_R349/U_Q15/U_R341 for MOR comment.
P.25 [VGA (Memory BUS) 4/6]Change R5795/R5796/R5809/R5810 to 40.2 ohm for AMD comment.
P.34 [CRT]NC R5752 for no need of semi-PNP function.

(2009/09/12)

P.80 [VGA Power (ATI_VDD)] Change PC159/PC160 to 1C-2B20105-K100(NC) for more stability.
P.01 [Index page]Update information.
P.02 [BLOCK DIAGRAM]Update information.
P.10 [PCH (HDA,JTAG,SAT)]Update SPI ROM information.
P.49 [eSATA Combo Conn.]Del F10 for no need.
P.49 [LVDS Connector]Add F15/L99 to follow M870.
P.10 [PCH (HDA,JTAG,SAT)]Add 100K pull-low resistors R5969/R5970/R5971 on SPI0_MOSI/SPI0_CLK/SPI0_CS# for Intel EDS request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R943/R974/R982/R1626 to 1R-0000103-J200.
P.63 [AUDIO (MUTE)*]Change U_R340/U_R350/U_R663 to 1R-0000103-J200.
P.62 [AUDIO (CODEC)*]Change U_R652/U_R662 to 1R-0000103-J200.
P.52 [Camera Connector]Add R5972/F16 for adding fuse solution.
P.25 [LVDS Connector]NC CN13 Pin1/Pin5/Pin6 for del EDID function.
P.24 [VGA (I/O) 3/6]NC U204B ATI_LVDS_SCL/ATI_LVDS_SDA for del EDID function.
P.20 [DDRIII(SO-DIMM_0) 1/2]NC CAP13 for no need.
P.21 [DDRIII(SO-DIMM_1) 2/2]NC CAP22 for no need.
P.25 [VGA (Memory BUS) 4/6]Change Madison/Park description.
P.25 [VGA (Memory BUS) 4/6]NC R5806/R5807/R5808 for AMD comment.
P.63 [AUDIO (CODEC)*]Change the setting to ALC269 (NC: U_C441/R5943/U_R5789, Stuff U_C930/R5944/U_R5790).
P.71 [DCIN&Charger]Change PL3 to NC for costdown.
P.75 [VTT&PCH Power(+1_05V)]Change PR44 from 0ohm to 2.2ohm for vendor suggest.
P.76 [DDR3 Power (+1_5V/+0_75V)]Change PR39 from 0ohm to 2.2ohm for vendor suggest.
P.80 [VGA Power (ATI_VDD)]Change PR549 from 0ohm to 2.2ohm for vendor suggest.

P.57 [Touch Pad]Del F12 for no need.
P.35 [LVDS]Update Panel ID information.
P.51 [AUDIO (CODEC)*]Change U_C787/U_C476/U_C459 to 1C-2B20103-K200.
P.28 [VRAM(DDR3)# 1/4]Change C6303 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.29 [VRAM(DDR3)# 2/4]Change C6304 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.30 [VRAM(DDR3)# 3/4]Change C6257 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.31 [VRAM(DDR3)# 4/4]Change C6258 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.28 [VRAM(DDR3)# 1/4]Change C4028/C4036 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.80 [VGA Power(ATI_VDD)]Change PC172 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.77 [SYS Power(+1_8V)]Change PC247 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.65 [AUDIO (Power)*]Change U_C467 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
P.50 [PCIE (MS) 1/2]Change R5912/R5913/R5914/R5911/R5915/R5916/R5917/R5918 /R5919 to 33ohm for correcting SI test fail.
P.51 [PCIE (SD) 2/2]Change R5920/R5921/R5922/R5923/R5924 to 33ohm for correcting SI test fail.

(2009/09/13)

P.34 [CRT]Change CN20 to DZ11A91-SB281-4H for different package.
P.68 [AUDIO (Ext MIC Jack)*]Change U_CN5 to JA63331-R1T0-7H for ME request.

(2009/09/14)

P.45 [LAN (88E8059) 1/2]Change C995 to 10uF for Marvell comment.
P.74 [SYS Power (+3_3V/+5V)] Change PR122/PR201 to 2.2 ohm for RF noise.
P.78 [CPU Power_VHCORE] Change PR563 to NC, change PU28 pin25 connect to PROCHOT# for design change.
P.04 [ARD (CLK,MISC,JTAG)]Add off-page PROCHOT#.
P.54 [Felica Connector]NC R5963/F14, stuff C869/U48/R630/C845/R5964 for Felica fuse solution fail.
P.49 [eSATA Combo Conn.]Add R5974/R5975/R5976/R5977 to reduce the trace length on U214 for vendor request.

(2009/09/15)

P.11 [PCH (PCI-E,SMBUS,CLK)]Make R902/R903 from +3VRUN pull-high to +3VALW pull-high for Intel recommendation.
P.38 [HDMI]Change CN21 to DF03-577-1931.

(2009/09/16)

P.14 [PCH (PCI,USB,NVRAM)]NC R1466 for Intel Braidwood disable guideline.

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(2009/09/19)

P.25 [VGA (Memory BUS) 4/6]Change R5805 to 10k
for AMD comment.
P.25 [VGA (Memory BUS) 4/6]Add R5981 pull-high to +3VRUN on TESTEN
for AMD hang-up workaround.
P.24 [VGA (I/O) 3/6]Add R5978 pull-low to GND on ATI_JTAG_RST
for AMD hang-up workaround.
P.24 [VGA (I/O) 3/6]Add R5979 pull-high to +3VRUN on ATI_JTAG_TMS
for AMD hang-up workaround.
P.24 [VGA (I/O) 3/6]Add R5980 between R_XTALSSIN and ATI_JTAG_TCLK
for AMD hang-up workaround.

(2009/11/04)

P.07 [ARD (GRAPHICS POWER)] Delete PJ43 for redundant design of
EVT & DVT
P.34 [CRT] Add F17 for current limit by MOR comment
P.74 [SYS Power (+3_3V/+5V)] Delete PJ11 and PJ12 for redundant
design of EVT & DVT
P.75 [VTT&PCH Power(+1_05V)] Delete PJ22 and PJ23 for redundant
design of EVT & DVT
P.76 [DDR3 Power(+1_5V/+0_75V)] Delete PJ26 and PJ27 for redundant
design of EVT & DVT
P.77 [SYS Power(+1_8V)] Delete PJ36 for redundant design of EVT & DVT
P.78 [CPU Power_VHCORE] Change PC112 from 68u_25V to
OS_Con cap 47u_25V by MOR request
P.80 [VGA Power(ATI_VDD)] Delete PJ31 and PJ37 for redundant
design of EVT & DVT

(2009/11/12)

P.25 [VGA (Memory BUS)] Change R5805 to NC & Mount R5981 for AMD suggestion
P.39 [EC+KBC(NPCE783L)] Add R5982 on OVT_EC# for GPIO70 need pull high
P.62 [SWITCH (Botton & KB LED)*] Exchange function name for Assist &
Web button
P.35 [LVDS] No mount R5940 to cancell Instant_On function by MOR request
P.39 [EC+KBC(NPCE783L)] No mount R5851 to cancell Instant_On function
by MOR request
P.55 [Status LED & LID] R689 change resistor value to 300 Ohm, R692 change
resistor value to 909 Ohm, R693 change value to 300 Ohm, R5945~R5947
change resistor value to 392 Ohm for LED brightness by MOR request
P.37 [LVDS Connector] Change CN13 to 1N-004000E-FKG0 for better L6 process
P.40 [KB Connector] Add TP1233,TP1234 for BFT test
P.35 [LVDS] Add TP1231,TP1232 for BFT test
P.51 [PCIE(SD) 2/2] Add TP1239,TP1240 for BFT test
P.57 [Touch Pad] Add TP1245~TP1250 for BFT test
P.54 [Felica Connector] Add TP1241~TP1244 for BFT test

(2009/11/16)

P.71 [DCIN&Charger] Change pc126 from 1000P_50V_0603_X7R to 1000pF_50V_0402_X7R
for MOR request
P.78 [CPU Power_VHCORE] Change pc253 from 1000P_16V_0402_X7R to
1000pF_50V_0402_X7R for MOR request
P.82 [OVP protection] Change pc41 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R
for MOR request
P.10 [PCH (HDA,JTAG,SAT)] Update U43 schematic symbol
P.73 [Identify IC] Update PU5 schematic symbol
P.52 [Camera Connector] L93,L94 change to Bead,MAX ECHO,EBMS100505A121 0.5A,
120ohm/100MHz,25%,0402(1005mm) by MOR request
P.67 [Audio] U_L4,U_L5 change to Bead,MAX ECHO,EBMS100505A121 0.5A,
120ohm/100MHz,25%,0402(1005mm) by MOR request
P.45 [LAN (88E8059) 1/2] C6077 change to SMD,MLCC,X7R,1000pF,50V,10%,0402
by MOR request
P.63 [AUDIO (CODEC)*] U_C440 change to SMD,MLCC,X7R,1000pF,50V,10%,0402
by MOR request
P.46 [LAN (Transformer) 2/2] C568 change to SMD,MLCC,X7R,1000pF,50V,10%,0402
by MOR request
P.57 [Touch Pad] C130,C133 change to SMD,MLCC,NPO,47pF,50V,5%,0402
by MOR request
P.39 [EC+KBC(NPCE783L)] C22 change to SMD,MLCC,NPO,22pF,50V,5%,0402
by MOR request
P.50 [PCIE (MS) 1/2] C544,C785,C786 change to SMD,MLCC,NPO,22pF,50V,5%,0402
by MOR request
P.63 [AUDIO (CODEC)*] U_C439 change to SMD,MLCC,NPO,22pF,50V,5%,0402
by MOR request
P.64 [AUDIO (MUTE)*] U_R351 change to SMD,RES,200K,1/16W,5%,0402
by MOR request
P.64 [AUDIO (MUTE)*] U_R352 change to SMD,RES,33K,1/16W,5%,0402
by MOR request
P.64 [AUDIO (MUTE)*] U_R341,U_R349, change to SMD,RES,10K,1/16W,5%,0402
by MOR request
P.10 [PCH (HDA,JTAG,SAT)] R5905, change to SMD,RES,51ohm,1/16W,5%,0402
by MOR request
P.39 [EC+KBC(NPCE783L)] RP1,RP20,RP90 change to SMD,RES,10K,1/16W,5%,0402
and locations are R5991~R5996 by MOR request
P.39 [EC+KBC(NPCE783L)] RP21, change to SMD,RES,2.2K,1/16W,5%,0402
and locations are R5987,R5988 by MOR request
P.39 [EC+KBC(NPCE783L)] RP22, change to SMD,RES,4.7K,1/16W,5%,0402
and locations are R5989,R5990 by MOR request
P.43 [Express Card] Update U42 Schematic symbol
P.55 [Status LED & LID] Change TP1224~TP1230 to top for BFT test

(2009/11/17)

P.83 [HOLE & AMI LABEL] Add BOSS2 for M960 wireless card use only
P.44 [Mini-PCIE Card (WLAN)] Add TP1235~TP1238 on BT_WLAN_SW# &
GND for BFT test
P.45 [LAN (88E8059) 1/2] LAN chip 88E8059 change packing method to
tapping for better L6 process
P.24 [VGA (I/O) 3/6]Connect a stable clock source (from clock gen SS 27MHz) to
GPIO26_TCK.
Add 5991 pull-down with 10K ohm to ground for the Park/Madison JTAG test
block intermittently fails to initialize correctly. Incorrect
initialization may result in a failure to boot.
P.35 [LVDS] SW1 change from 12-pin to 8-pin panel ID SW
P.15 [PCH (GPIO,VSS_NCTF,RSVD)] NC_R5931 & move R5939 from P.35
to P.15
P.39 [EC+KBC(NPCE783L)] Move R5940 from P.35 to P.39

(2009/11/18)

P.57 [Touch Pad] Add F12 for cable short test fail
P.35 [LVDS] Add test point from TP1251~TP1260 for panel ID switch BFT test
P.58 [Thermal Sensor] Delete VGA thermal sensor function, NC_U26,
NC_R946, NC_C534, NC_C547 because GPU support DTS function
P.25 [VGA (Memory Bus) 4/6] Change R5878 resistor value from
680 Ohm to 51 Ohm for memory reset circuit update from AMD
P.55 [Status LED & LID)] Change U21 to E-CMOS EC2618NLB1GR
for distance can't meet MOR spec

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M960/M970 PVT

(2009/11/19)

P.24 [VGA (I/O) 3/6] Add TP1261,TP1262 on GPIO8 & GPIO 22 for reserve AMD errata solution
P.11 [PCH (PCI-E,SMBUS,CLK)] Reserve R5992~R6000 for Intel FCIM function
P.78 [CPU Power_VHCORE] Change PR554 and PR558 from 0ohm to 2.20hm for EMI request
P.80 [VGA Power(ATI_VDD)] Change PR183 from 15.4k to 15k for VGA Park high level request
change PR210 from NC_7.15K to 68k for VGA Madison high level request

(2009/11/20)

P.24 [VGA (I/O) 3/6]Delete R5978,R5979,R5980 for needless
P.24 [VGA (I/O) 3/6]NC R5991 and add R6001(NC) for AMD Errata suggestion
P.25 [VGA (Memory BUS]NC R5981 for AMD Errata suggestion
P.15 [PCH]Change R5939 to mount for Panel ID setting requirement
P.64 [Audio(Mute)]Change U_R364 from 33kohm to 3.3kohm for satisfy hFE under 100 as MOR's suggestion.
P.45 [LAN]Change R84 from 4.7kohm to 0ohm for vendor modification

(2009/11/21)

P.24 [VGA]Add R6002,R6003,Y9,C6342,C6343 and NC them, it reserve for Intel FCIM function.
P.69 [Audio (USB)*]Change the footprint of U_CN2,U_CN3,U_CN6 as SMT suggestion.
P.42 [Debug Port]Add C6344 for EMI request.
P.66 [AUDIO]Add C6345 for EMI request.
P.46 [LAN]Change L47 from 100R to 300R for EMI request.
P.71 [DCIN&Charger]: Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf , PC577 4700pf for EMI request
P.74 [SYS Power (+3_3V/+5V)]:Add PC578 and PC579 680pf near PQ70 for EMI request
P.78 [CPU Power_VHCORE]:change PC151 and PC156 from NC to mount 0.1uf for EMI request
P.81 [Others power plane]:Add PC584 680pf,PC585 0.1uf near PQ26 for EMI request.

(2009/11/22)

P.60 [Audio]Add C6348~C6351 for speaker noise issue.
P.10 [PCH]Add C6352,C6353 and NC them, reserve for EMI request.
P.63 [AUDIO]NC U_C439 and add U_C931(NC) for EMI request.
P.55 [LED]Change R5945,R5946,R5947 from 392ohm to 649ohm and R390 from 120ohm to 261ohm as DQA&ME request.
P.63 [Audio]Change U_R668,U_R665,U_R660,U_R670,U_R672,U_R659(22ohm) from 0402 to 0201 for implement ME solution and layout space is not enough.
And change U_R667,U_R664(33kohm), and R5943(NC),R5944(0ohm), and U_R339(20kohm), and U_R338(39.2kohm), and U_R652,U_662(10kohm) from 0402 to 0201 for implement ME solution and layout space is not enough.

(2009/11/23)

P.39 [EC]Delete R5983,R5984 and add RP20 for layout space concern
P.81 [Other power plane]Change PR661 from 0603 to 0402 for MOR request to cost down.
P.15 [PCH]Delete RP19 and add R6004,R6005,R6006 for MOR request to cost down.
P.52 [Camera]Change C9 from 1C-2Y70106-Y001 to 1C-2Y70106-Y000 for MOR request to cost down.
P.64 [Audio]Change U_Q20 form 2N7002W to SRK7002 for ESD issue.
P.25 [VGA]Change R5805 from NC to mount for AMD suggestion.
P.83 [HOLE]Change H30,H29,H8,H10,H4 hole size as ME's request.
P.34 [CRT]Change CN20 from FOX_DZ11A91-SB281-4H to FOX_DZ11AE1-SB1SD-4H as ME's request.
P.61 [Audio/USB DB CONN]Change CN31 from FOX_GB5RF500-1203-7H to FOX_GB5RF500-1203-8H for ME's request.
P.66 [Audio (Audio/USB CONN)*]Change U_CN1 from FOX_GB5RF500-1203-7H to FOX_GB5RF500-1203-8H as ME's request.
P.54 [Felica]Change CN7 from FOX_GB5RF060-1203-7H to FOX_GB5RF060-1203-8F as ME's request.

(2009/11/23)

P.57 [TouchPad]Change CN8 from FOX_GB5RF060-1203-7H to FOX_GB5RF060-1203-8F as ME's request.
P.10 [PCH]Change C6352 from 0.1uF to 33pF(mount) and R618 from 33ohm to 47ohm as EMC request.
P.81 [Other power plan]Change PC188 from 10uF to 1uF(mount) for improve power signal.
P.63 [Audio]Change U_R661,U_R671,U_R676,U_673,U_R321 from 0402 to 0201 for layout space concern.

(2009/11/24)

P.25 [VGA]Change R5805 from 10k to 5.1k as AMD's suggestion
P.35 [LVDS]Change SW1 from DHNF-04-T-Q-T-R_SW-SMD8P to DHNF-06-T-Q-T/R_SW-SMD12 for shortage issue.

(2009/11/28)

P.74 [SYS Power]Change PC578,PC579 from 1C-2B20681-M000 to 1C-2B20681-K000 for PUR's suggestion.
P.46 [LAN]Change L47 from 1L-BACMS16-0809 to 1L-BTB1608-080D for PUR's suggestion.
P.42 [Debug Port]NC CN30 for EMC solution.
P.41 [SPI Flash ROM]NC U3,R43,C20 and mount R775 for EMC solution.
P.80 [VGA Power(ATI_VDD)]:
1.PR183=10.5k for VGA M92 XT high voltage level request
2.PR183=10.5k for VGA M92 XTX high voltage level request
3.PR183=34.8k for VGA M96 high level request
4.PR183=75k for VGA madision high level request
5.PR183=15K for VGA Park high level request
6.NC PR210

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M960/M970 MP

(2009/12/22)

P.76 [DDR3 Power(+1_5V/+0_75V)] Mount PQ59, change PR600 resistor to 0 Ohm & no mount PR145 to change the enable signal to RUN_PWRGD by MOR request.
P.38 [HDMI] Change CN21 symbol from 2N-0019007-MKG0 to 2N-0019003-MKG0 to improve factory process

(2009/12/23)

P.80 [VGA Power(ATI_VDD)] 1.PR222=39.2k for VGA M92 XTX 1.0VPEG 1.1V voltage request
2.PR222=27k for VGA Park 1.0VPEG 1.0V voltage request
3.PR222=27k for VGA Madison 1.0VPEG 1.0V voltage request
P.25 [VGA (Memory Bus 4/6)] 1.R5795, R5796, R5809, R5810=100 for VGA M92XTX voltage reference
2.R5795, R5796, R5809, R5810=40.2 for VGA Park voltage reference
3.R5795, R5796, R5809, R5810=40.2 for VGA Madison voltage reference
P.83 [HOLE & AMI LABEL] Mount AMI label for AMI certifcate
P.10 [PCH (HDA,JTAG,SAT)] No mount CN18, U43, C815, R542 & Mount R1551 for needless in MP
P.64 [AUDIO (MUTE)*] Change U_Q15 with ESD protection for factory ESD issue

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(2009/12/24)

P.83 [HOLE & AMI LABEL]Delete BOSS2 for needless from ME's request
P.46 [LAN(Transformer)]Change L70 from LANKOM to DELTA for LANKOM transformer issue in PVT
P.45 [LAN]Add R6010 reserve for 8057 solution
P.04 [ARD]Delete R937,R930 for MOR's request
P.06 [ARD]Delete R860 for MOR's request
P.24 [VGA]Delete R5785,R5788,R5789 for MOR's request
P.39 [EC]Delete R39,R46 for MOR's request
P.44 [Mini-PCIE Card]Delete R5901 for MOR's request
P.57 [Touch Pad]Delete R5869,R5868 for MOR's request

(2009/12/28)

P.10 [PCH]Change R618 from 47ohm to 68ohm and Change C6353 from NC_0.1uF to mount 22pF for EMC audio FFC issue
P.63 [Audio]Change U_R326 from 22ohm to 0ohm for EMC audio FFC issue

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